AK4201

Stereo Cap-less HP-Amp

GENERAL DESCRIPTION

The AK4201 is an audio stereo cap-less headphone amplifier. The AK4201 eliminates the need for large DC-blocking capacitors with a built-in Charge-pump circuit. A 100dB PSRR (Power Supply Rejection Ratio) is achieved by a built-in regulator, and 2Vrms outputs are available with excellent linearity when the AK4201 is used as a lineout amplifier. The AK4201 is available in tiny 12-pin USON (2.2 X 2.9mm), saving board space, cost, and reducing component height.

FEATURE

- ☐ **Stereo Cap-less Amplifier (No DC-blocking capacitors required)**
- ☐ **High PSRR (100dB at 217Hz)**
- ☐ **Output Power:**
  - **65 mW x 2ch @ 16Ω, AVDD=PVDD=5.0V, THD+N=-60dB**
  - **30 mW x 2ch @ 16Ω, AVDD=PVDD=3.3V, THD+N=-60dB**
- ☐ **Output Noise Level: 11µVrms (Ri=20kΩ, Rf=30kΩ)**
- ☐ **Line-Out level:**
  - **2.0Vrms @ 5kΩ, AVDD=PVDD=5.0V**
  - **2.0Vrms @ 5kΩ, AVDD=PVDD=3.3V**
- ☐ **Regulator built-in**
- ☐ **THD+N**:
  - **-60dB @ 16Ω, 50mW, AVDD=PVDD=5.0V**
  - **-60dB @ 16Ω, 20mW, AVDD=PVDD=3.3V**
  - **-100dB @ 5kΩ, 2Vrms, AVDD=PVDD=5.0V**
  - **-100dB @ 5kΩ, 2Vrms, AVDD=PVDD=3.3V**
- ☐ **Low Power Shutdown Mode**
  - **0.1µA (typ)**
- ☐ **Mute function at shutdown mode:**
  - **-88dB attenuation**
  - **No external component is required**
- ☐ **Zero offset by ground-referenced output**
- ☐ **Pop noise free at power-ON/OFF**
- ☐ **Power Supply: 2.6V ~ 3.6V or 4.5V ~ 5.5V**
- ☐ **Ta: –40 ~ 85°C**
- ☐ **Package: 12pin USON (2.2 x 2.9mm, 0.5mm pitch)**

■ Block Diagram

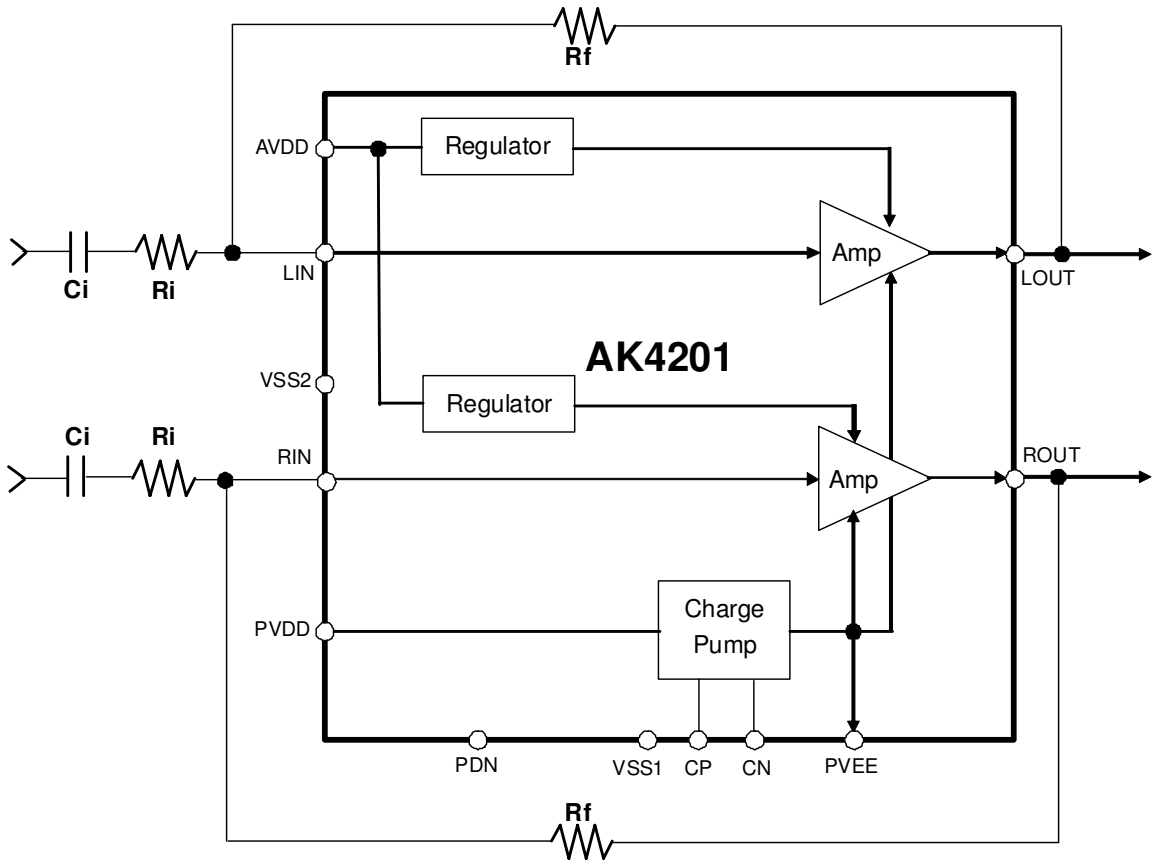
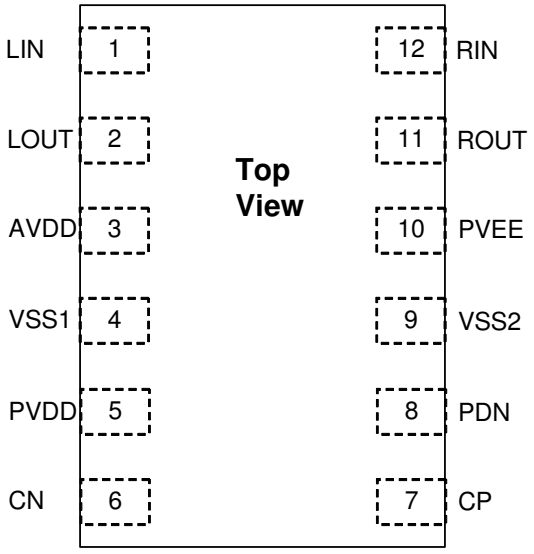


Figure 1. AK4201 Block Diagram

■ Ordering Guide

AK4201EU	–40 ~ +85°C	12pin USON (2.2mm x 2.9mm, 0.5mm pitch)
AKD4201	Evaluation board for AK4201	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LIN	I	L-channel analog input
2	LOUT	O	L-channel analog output
3	AVDD	-	Headphone positive power supply pin
4	VSS1	-	Ground 1 pin
5	PVDD	-	Charge-pump positive power supply pin
6	CN	I	Negative charge-pump capacitor terminal pin
7	CP	O	Positive charge-pump capacitor terminal pin
8	PDN	I	Power-down mode pin "H": Power-up, "L": Power-down
9	VSS2	-	Ground 2 pin
10	PVEE	O	Charge-pump circuit negative voltage output pin
11	ROUT	O	R-channel analog output
12	RIN	I	R-channel analog input

Note. The PDN pin must not be floated.

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Analog	LIN, RIN, LOUT, ROUT	Connect Output pin to Input pin when one channel is used and the other is not used. (Example) Connect the ROUT pin to the RIN pin if Rch is not used.

ABSOLUTE MAXIMUM RATINGS

(VSS1=VSS2 =0V (Note 1))

Parameter		Symbol	min	max	Units
Power Supplies: (Note 2)	Analog	AVDD	–0.3	6.0	V
	Charge Pump	PVDD	–0.3	6.0	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Input Voltage (Note 3)		VIN	–0.3	(AVDD + 0.3) or 6.0	V
Ambient Temperature (powered applied)(Note 4)		Ta	–40	70(Note 5) 85(Note 6)	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages are respect to ground. The PDN pin should be held to "L" when powered-up, and it should be set to "H" after all power supplies are powered-up. The PDN pin should be held to "L", when powered-down.
Note 2. VSS1 and VSS2 must be connected to the same analog plane.
Note 3. LIN, RIN and PDN pin
The maximum value is smaller value between (AVDD+0.3)V and 6.0V.
Note 4. PCB wiring density should be 150% or more. Device back PAD should be connected to ground.
Note 5. Headphone Output Power should below 65mW/ch.
Note 6. Headphone Output Power should below 50mW/ch.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1=VSS2 =0V (Note 1))

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 7)	Analog, Charge Pump	AVDD, PVDD	4.5 2.6	5.0 3.3	5.5 3.6	V
	Difference	AVDD – PVDD	-0.3	0	0.3	V

Parameter	Symbol	min	typ	max	Units
External Input Resistance	Ri	10	-	100	kΩ
External Feedback Resistance	Rf	10	-	100	kΩ
Gain Range	Gain	-16	-	16	dB
Load					
Resistance (LOUT, ROUT pins)	R_L	16	-	-	Ω
Capacitance (LOUT, ROUT pins)	C_L	-	-	300	pF
Capacitance (LIN, RIN pins)	Csum	-	-	20	pF

Note 7. AVDD and PVDD must not be in the range from 3.6V to 4.5V.

Note: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS (AVDD=PVDD=5.0V)

(AVDD=PVDD=5.0V; PDN=5.0V; Ta=25ºC; VSS1=VSS2=0V; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Gain=+3.5dB (Ri=20kΩ, Rf=30kΩ); Headphone-Amp: R_L =16Ω; Charge Pump Circuit External Capacitance: C1=C2= 1μF (Figure 3), unless otherwise specified)

Parameter	min	typ	max	Units
Output Power				
R_L =16Ω, 0.68Vrms Input	-	65	-	mW
THD+N				
0.68Vrms Input; Po = 65mW @ R_L =16Ω	-	–60	-	dB
0.60Vrms Input; Po = 50mW @ R_L =16Ω	-	–60	-50	dB
1.33Vrms Input; Vo = 2.0Vrms @ R_L =5kΩ	-	–100	-90	dB
S/N (Signal-to-Noise Ratio)				
R_L =16Ω (A-weighted) (Note 8)	94	100	-	dB
R_L =5kΩ (A-weighted) (Note 9)	100	106	-	dB
PSRR (Power Supply Rejection Ratio) (Note 10)				
217Hz	-	100	-	dB
1kHz	-	90	-	dB
Interchannel Isolation				
R_L =16Ω	60	80	-	dB
R_L =5kΩ	-	100	-	dB
Output Offset Voltage	-	±0	±1	mV
Start-up time (Note 11)	-	-	50	ms
Power Supplies				
AVDD + PVDD (Normal Mode; No Output)	-	4.8	7.2	mA
AVDD + PVDD (Power-Down Mode, PDN =0V)	-	0.1	10	uA

Note 8. In case of 0.68Vrms Input (Po=65mW).
Note 9. In case of 1.33Vrms Input (Vo=2Vrms).
Note 10. PSR is applied to AVDD and PVDD with 300mVpp sine wave.
Note 11. The time from the PDN pin= “H” to when the AK4201 can output signals.

ANALOG CHARACTERISTICS (AVDD=PVDD=3.3V)

(AVDD=PVDD=3.3V; PDN=3.3V; Ta=25ºC; VSS1=VSS2=0V; Input Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Gain=+3.5dB (Ri=20kΩ, Rf=30kΩ); Headphone-Amp: R_L =16Ω; Charge Pump Circuit External Capacitance: C1=C2= 1μF (Figure 3), unless otherwise specified)

Parameter	min	typ	max	Units
Output Power				
R_L =16Ω, 0.46Vrms Input	-	30	-	mW
THD+N				
0.46Vrms Input; Po = 30mW @ R_L =16Ω	-	-60	-	dB
0.27Vrms Input; Po = 10mW @ R_L =16Ω		-60	-50	dB
1.33Vrms Input; Vo = 2.0Vrms @ R_L =5kΩ	-	-100	-90	dB
S/N (Signal-to-Noise Ratio)				
R_L =16Ω (A-weighted) (Note 12)	90	96	-	dB
R_L =5kΩ (A-weighted) (Note 13)	100	106	-	dB
PSRR (Power Supply Rejection Ratio) (Note 14)				
217Hz	-	70	-	dB
1kHz	-	70	-	dB
Interchannel Isolation				
R_L =16Ω	60	77	-	dB
R_L =5kΩ	-	100	-	dB
Output Offset Voltage	-	±0	±1	mV
Start-up time (Note 15)	-	-	50	ms
Power Supplies				
AVDD + PVDD (Normal Mode; No Output)	-	3.8	5.7	mA
AVDD + PVDD (Power-Down Mode, PDN =0V)	-	0.1	10	μA

Note 12. In case of 0.46Vrms Input (Po=30mW).
Note 13. In case of 1.33Vrms Input (Vo=2Vrms).
Note 14. PSR is applied to AVDD and PVDD with 100mVpp sine wave.
Note 15. The time from the PDN pin= “H” to when the AK4201 can output signals.

DC & SWITCHING CHARACTERISTICS

(Ta= -40 ~ 85°C; AVDD=PVDD=2.6 ~ 3.6V or 4.5 ~ 5.5V, Note 16)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	1.6	-	-	V
Low-Level Input Voltage	VIL	-	-	0.5	V
Input Leakage Current	Iin	-	-	±2	μA
Power-down (PDN pulse Width)	tPD	150		-	ns

Note 16. Apply to the PDN pin.

■ Timing Diagram

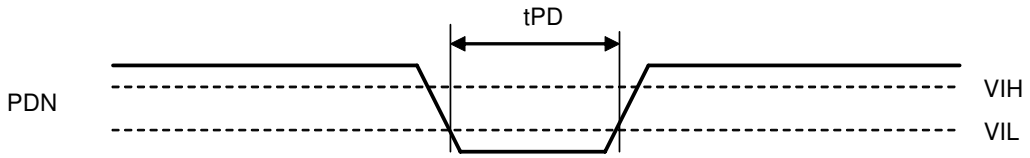


Figure 2. Power-down Timing

■ Charge Pump Circuit

The charge pump operates by the output of a regulator which uses PVDD voltage. The negative power supply (PVEE) for headphone amplifiers is generated from internal charge pump circuit. The external capacitors are showed in Figure 3. Low ESR (Equivalent Series Resistance) capacitors with 1uF to 2.2uF (+/-35% or less difference including temperature drift and a deviation over samples) are recommended for C1 and C2. The minimum value of capacitors should be more than 0.65uF if temperature drifts and a deviation over samples are big.

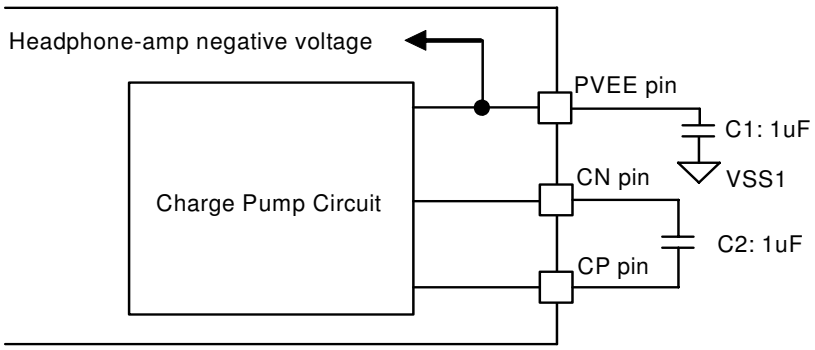


Figure 3. Charge Pump Circuit External Capacitor

■ Headphone-Amp (LOUT/ROUT pins)

Power supply voltage for headphone amplifiers is supplied by a regulator for positive power and a charge-pump for negative power. The headphone amplifier output is single-ended and centered on VSS1(0V). Therefore, a capacitor for AC-coupling can be removed. The minimum load resistance is 16Ω. The output impedance is 20Ω (typ) when powered-down.

■ Power-Up/Down Sequence

The PDN pin must keep “L” until all power supply pins (AVDD, PVDD) are supplied, and must be set to “H” after.

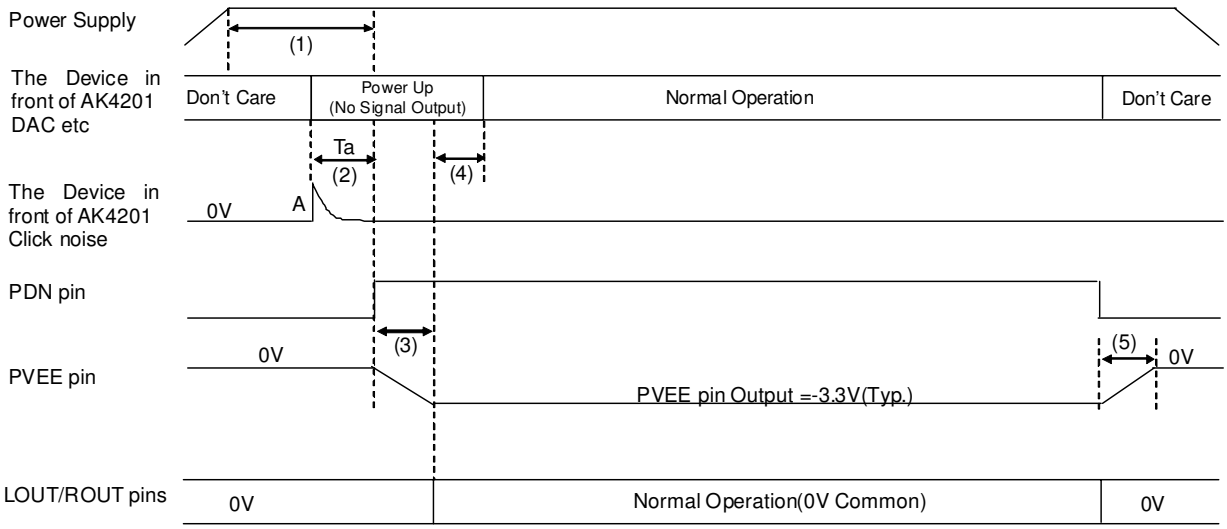


Figure 4. Power-up/down Sequence example

(1) The interval from power Up to PDN pin = “L” → “H”

“L” time of 150ns or more is needed to reset the AK4201.

The power should be ON when the PDN pin = “L”. The PDN pin should be set to “H” after power supply (AVDD, PVDD) are ON.

(2) The interval from power-up of the signal source device in front of the AK4201 to the AK4201’s PDN pin transition from “L” to “H”

The other device should be powered up with no signal (e.g. MUTE). When a step wave (an instant DC level change) is output from the other device at the power-up, a high pass filter response wave will occur at “A” timing of Figure 4, according to the time constant of the input coupling capacitor (Ci) and the input resistor(Ri) in front of the AK4201. In order to prevent this pop noise through the AK4201, a wait time “Ta” is required after the other devices are powered-up. The AK4201 can attenuate pop noises of the other device by a built-in mute circuit during shutdown mode (PDN pin= “L”).

Ta calculation example: (in the case of Ci =0.22uF, Ri = 20kΩ)

τ=0.22u * 20k = 4.4ms

Ta =τ* 7.6 = 33ms

(When noise level by former device= 2V, response wave level= 1mV. 7.6*τ is needed)

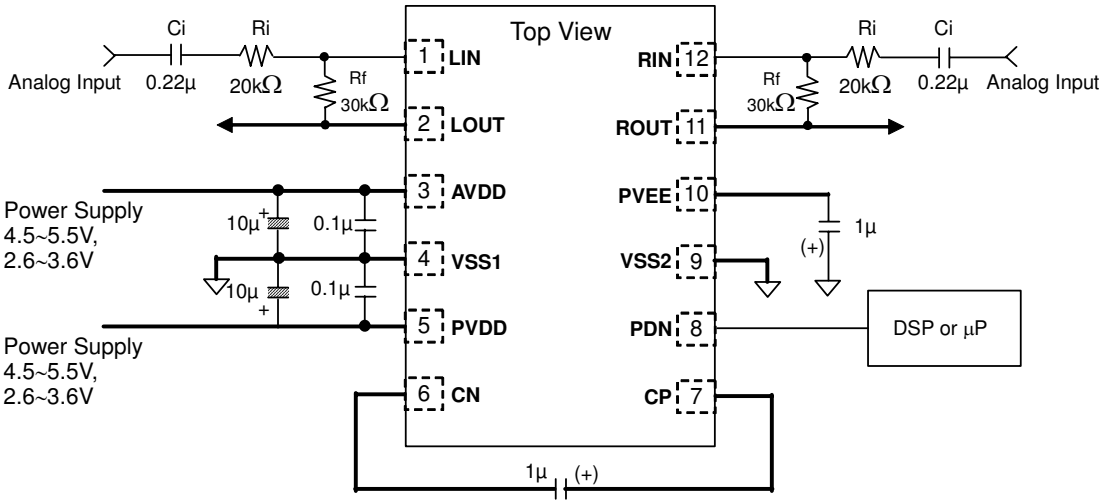
If a waiting time is not sufficient, a pop noise might occur, but there is no problem for the normal operation.

(3) The AK4201 is in normal operation 50ms (max) after the PDN pin goes to “H”. The other device in front of the AK4201 should be still muted during this interval (50ms).

(4) The other device in front of the AK4201 should start outputting the signal after the AK4201 starts Normal Operation. If click noise is generated by former device when MUTE is canceled, it will be output from the AK4201.

(5) The PDN pin = “L”. LOUT/ROUT pins short to VSS1 with 20Ω(typ.). After 50ms (max.), the PVEE pin will be 0V according to a capacitor which connected to PVEE and internal resistance (typ. 17.5kΩ). The AK4201 can be powered up again after 150ns or more from the PDN pin = “L”.

SYSTEM DESIGN



Note:

1. The PDN pin should be held to "L" when powered-up. The PDN pin should be set to "H" after all power supplies are powered-up. When power-down the AK4201, the PDN pin should be held to "L".

   Refer to "Power-Up/Down Sequence" to avoid pop noise when power-up/down the AK4201.
   1) Power-Up
      The power should be ON when the PDN pin = "L". The PDN pin should be set to "H" 150ns after all power supplies (AVDD, PVDD) are ON. 150ns "L" time or more is needed to reset the AK4201.
   2) Power-Down
      The AK4201 should be powered-down when the PDN pin = "L".

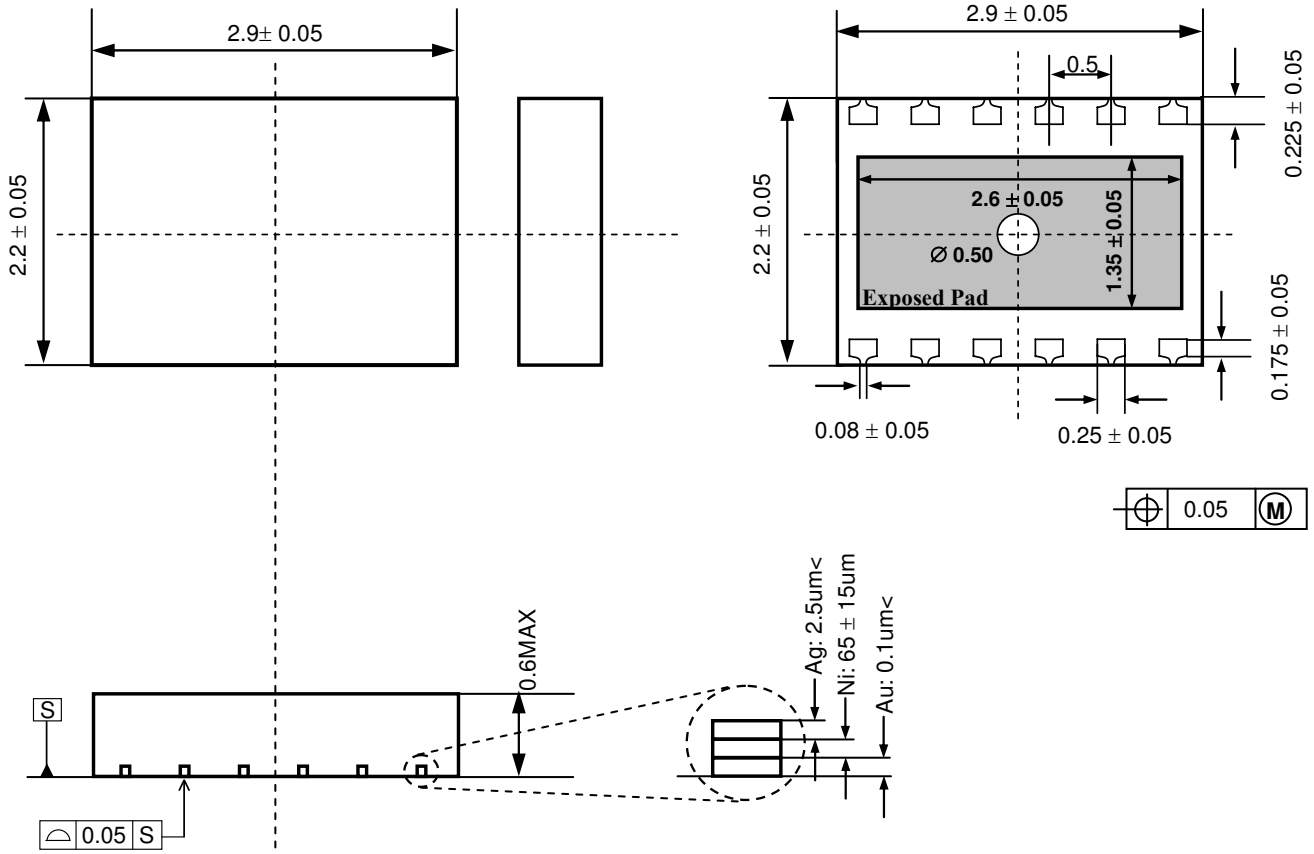
2. 1uF~2.2uF ceramic capacitors (±35% including temperature characteristics and piece-to-piece variations) should be connected to between the CP and CN pins, and the VSS1 and PVEE1 pins, respectively.

3. Both lines from the LIN pin and RIN pin to each Input resistance Ri and feedback resistance Rf should be as short as possible for better PSRR.

4. AC coupling capacitors should be connected to LIN and RIN pins, respectively.

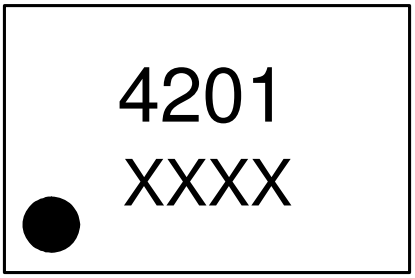
PACKAGE

12pin USON (2.2mm x 2.9mm, 0.5mm pitch)



Note) The exposed pad on the bottom surface of the package must be connected to the ground.

MARKING



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REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
09/05/12	00	First Edition		
11/02/03	01	Specification Addition	12	The package drawing was changed.

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