AK8160B2

Low Power & Low Jitter Clock Generator for PCI Express

1. General Description

The AK8160B2 is a member of AKM's low power and low jitter clock generator family designed for PCI Express generation 2.0. This device has one PLL with spread spectrum (SS) function and enables to output high quality differential 100MHz as PCI Express clock and 25MHz as reference simultaneously.

2. Features

- Low Current Consumption
  31mA Typ. (Full function, 25MHz output and 100MHz output)
- 25MHz Crystal Input or External Clock Input
- One single-end 25MHz-Reference Output without Spread Spectrum
- Two differential 100MHz Clock Outputs with Spread Spectrum
  Selectable Spread Spectrum ON / OFF
- Spread Spectrum Modulation ratio
  0% (Off), -0.5%
- Spread Spectrum Modulation frequency
  30kHz to 33kHz
- Low Jitter Performance of 100MHz Output Clock
  RMS Jitter: 2.6ps Max. (PCIE0p-1p/0n-1n pin, BW=10kHz – 1.5MHz)
  2.6ps Max. (PCIE0p-1p/0n-1n pin, BW=1.5MHz – 50MHz)
  Cycle to Cycle Jitter: 125ps Max. (PCIE0p-1p/0n-1n pin)
  23ps Typ. (1σ), (REFOUT pin)
- Supply Voltage
  3.0V – 3.6V
- Operating Temperature Range
  -40°C to +85°C
- Package
  0.4mm pitch 3mm x 3mm 20-pin QFN (Lead free)
- Application
  - DSLR : Digital Single-Lens Reflex camera
  - Network apparatus, Server, Datacenter
  - MFP : Multi-Function Printer
  - Game

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4. Block Diagram and Functions

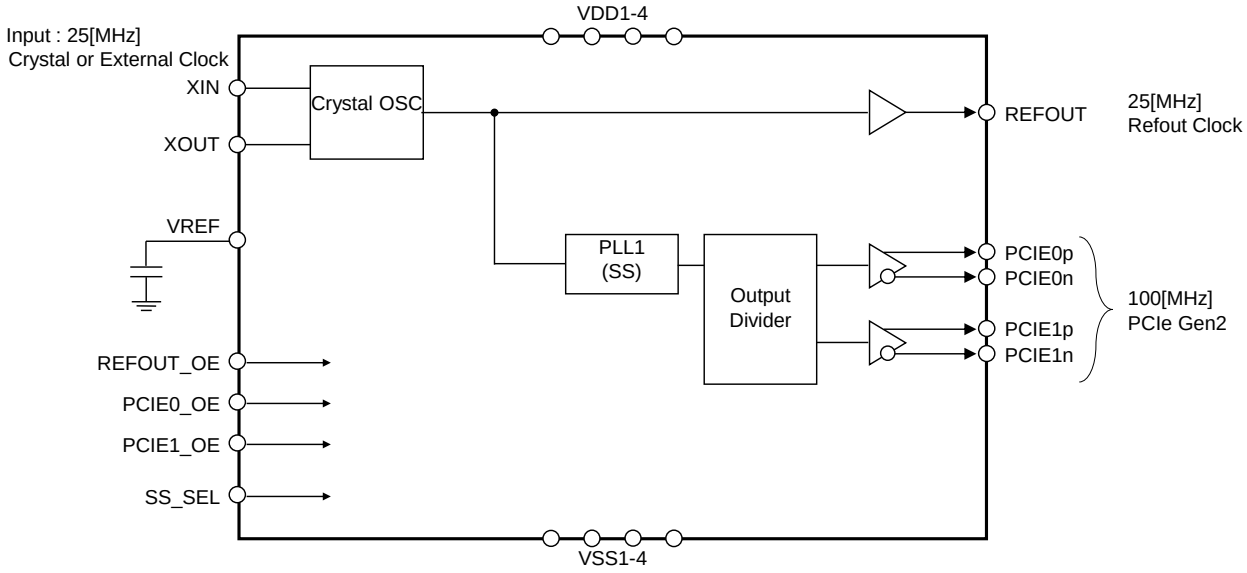


Figure 1. AK8160B2 Block Diagram

5. Pin Configurations and Functions

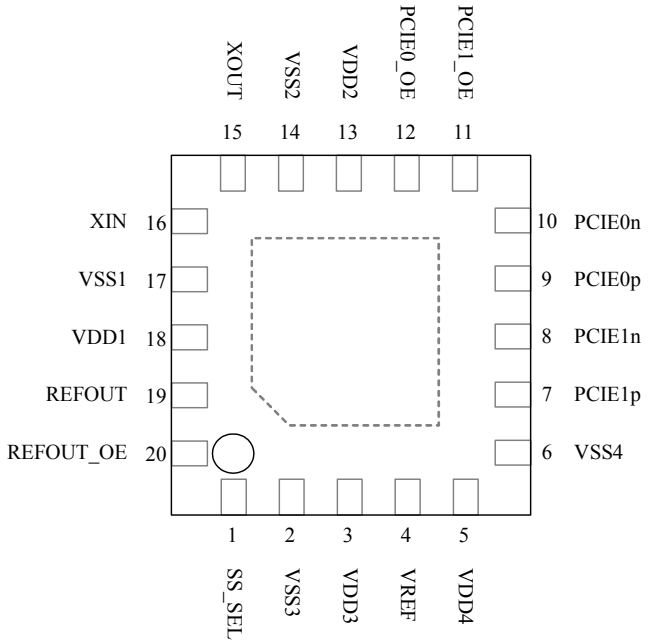


Figure 2. AK8160B2 Package: 20-Pin QFN (Top View)

Pin No.	Pin Name	Pin Type	Description
1	SS_SEL	DI	SS Modulation Control Pin This pin must be connected to “H” or “L”. SS_SEL = “L” : Modulation ratio is 0[%] (Off) SS_SEL = “H” : Modulation ratio is -0.5 [%]
2	VSS3	PWR	Ground pin 3
3	VDD3	PWR	Power Supply Pin 3
4	VREF	AO	Reference Voltage Generation Pin This pin must be connected to 1μF capacitor. This pin goes to Hi-Z when power down.
5	VDD4	PWR	Power Supply Pin 4
6	VSS4	PWR	Ground Pin 4
7	PCIE1p	DO	PCI Express Gen2 Clock Output pin 1 (Positive) This pin outputs 100MHz.
8	PCIE1n	DO	PCI Express Gen2 Clock Output pin 1 (Negative) This pin outputs 100MHz.
9	PCIE0p	DO	PCI Express Gen2 Clock Output pin 0 (Positive) This pin outputs 100MHz.
10	PCIE0n	DO	PCI Express Gen2 Clock Output pin 0 (Negative) This pin outputs 100MHz.

11	PCIE1_OE	DI	PCIE1p/n Output Control Pin This pin must be connected to “H” or “L”. PCIE1_OE = “L” : PCIE1p/n outputs “L”. PCIE1_OE = “H” : PCIE1p/n outputs 100MHz.
12	PCIE0_OE	DI	PCIE0p/n Output Control Pin This pin must be connected to “H” or “L”. PCIE0_OE = “L” : PCIE0p/n outputs “L”. PCIE0_OE = “H” : PCIE0p/n outputs 100MHz.
13	VDD2	PWR	Power Supply Pin 2
14	VSS2	PWR	Ground Pin 2
15	XOUT	AO	25MHz Crystal Connection Pin OPEN when an External Clock Input is used
16	XIN	AI	25MHz Crystal Connection Pin or External Clock Input Pin
17	VSS1	PWR	Ground Pin 1
18	VDD1	PWR	Power Supply Pin 1
19	REFOUT	DO	25MHz Output Pin
20	REFOUT_OE	DI	25MHz Output Control Pin This pin must be connected to “H” or “L”. REFOUT_OE = “L” : REFOUT outputs “L”. REFOUT_OE = “H” : REFOUT outputs 25MHz.
	Exposed Pad	---	Connecting exposed pad of package to board ground must be required.

Note:

AI : Analog input pin
AO : Analog output pin
DI : Digital input pin
DO : Digital output pin
PWR : Power supply and Ground pin

6. Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply voltage	VDD	-0.3 to 4.6	V
Input voltage	Vin	VSS-0.3 to VDD+0.3	V
Input current (any pins except supplies)	I_{IN}	±10	mA
Storage temperature	Tstg	-65 to 150	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKM recommends that this device is handled with appropriate precautions.

7. Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating temperature	Ta		-40		85	°C
Supply voltage (1)	VDD	Pin: VDD1 - 4	3.0	3.3	3.6	V
Output Load Capacitance	Cpl	Pin: REFOUT			25	pF

Note:

(1) Power to VDD1 – VDD4 requires to be supplied from a single source. A decoupling capacitor of 0.1µF for power supply line should be connected close to each VDD pin.

8. Electrical Characteristics

Current Consumption

All specifications at VDD: over 3.0V to 3.6V, Ta: -40 to +85°C, 25MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Current Consumption 1	$I_{DD}1$	(1), (2)		31	38	mA
Current Consumption 2	$I_{DD}2$	(1), (3)		30	37	mA
Current Consumption 3	$I_{DD}3$	(1), (4)		0	100	μA

Note:
(1) REFOUT : No load, PCIE0p/n, PCIE1p/n : CL=2[pF]
(2) Full function REFOUT output, 100MHz output
*REFOUT_OE = PCIE0_OE = PCIE1_OE = SS_SEL = "H"
(3) REFOUT output off, 100MHz output
*REFOUT_OE = "L", PCIE0_OE = PCIE1_OE = SS_SEL = "H"
(4) Full power down
* REFOUT_OE = PCIE0_OE = PCIE1_OE = "L"

DC Characteristics

All specifications at VDD: over 3.0V to 3.6V, Ta: -40 to +85°C, 25MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}	REFOUT_OE pin PCIE0_OE pin PCIE1_OE pin SS_SEL pin	0.7*VDD			V
Low Level Input Voltage	V_{IL}	REFOUT_OE pin PCIE0_OE pin PCIE1_OE pin SS_SEL pin			0.3*VDD	V
Input Leakage Current	I_L	REFOUT_OE pin PCIE0_OE pin PCIE1_OE pin SS_SEL pin	-1		+1	μA
VREF Output Voltage	V_{REF}	VREF pin C_{VREF} = 1μF	0.72	0.8	0.88	V
High Level Output Voltage	V_{OH}	REFOUT pin I_{OH} = -4mA	0.8*VDD			V
Low level Output Voltage	V_{OL}	REFOUT pin I_{OL} = 4mA			0.2*VDD	V

AC Characteristics (except Differential Output)

All specifications at VDD: 3.0V to 3.6V, Ta: -40 to +85°C, 25MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Clock Frequency	F_{in_xo}	XIN pin XOUT pin		25.000		MHz
Oscillation Accuracy	$F_{accuracy}$	REFOUT pin (1)	-30	0	+30	ppm
External Clock Frequency	F_{in_ext}	XIN pin (2)		25.000		MHz
Input Clock Voltage Swing	V_{swing_ext}	XIN pin (2)	1		VDD	Vpp
Input Clock Duty Cycle	$T_{extindc}$	XIN pin (2)		50		%
Output Frequency	F_{osc}	REFOUT pin		25.000		MHz
Output Rising and Falling	T_{RF}	REFOUT pin (3)		1.8	5.0	ns
Output Clock Duty Cycle	T_{outdc_xtal} (4)	REFOUT pin	45	50	55	%
	T_{outdc_ext} (5)	REFOUT pin	40	50	60	%
Cycle to Cycle Jitter	Jit_{c2c}	REFOUT pin (6)		23	48	ps
Output Lock Time	T_{lock}	REFOUT pin (7)		0.5	2	ms

Note:

(1) Specification of Frequency Accuracy is measured by connecting the standard 25MHz crystal unit for part number XRCGB25M000F3M00R0 of Murata Manufacturing Co., Ltd. on page 11.
This Output Clock Frequency Accuracy does not include accuracy of crystal unit.
Total output clock frequency accuracy could be up to “Output Clock Frequency Accuracy” + “Crystal unit accuracy”.

(2) Use Case of External Clock Input

(3) Transition time between 0.2VDD and 0.8VDD

(4) When the standard 25MHz Crystal Unit is connected.

(5) When the Duty Cycle of External Clock Input is 50%.

(6) 1σ in 10000 sampling or more

(7) Transition time to settle output into ±0.1% of specified frequency after escaping power down mode. (REFOUT_OE pin = PCIE0_OE pin = PCIE1_OE pin = ‘L’).

AC Characteristics (Differential Output pin : PCIE0p-1p/0n-1n pin)

All specifications at VDD: over 3.0V to 3.6V, Ta: -40 to +85°C, 25MHz Crystal, unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Average Output Frequency	F_{in}	SS Off (1)	99.97	100.000	100.03	MHz
		SS On (1)	99.47		100.03	MHz
Output Skew	T_{slew}				250	ps
Slew Rate of Output Rising and Falling	T_{slew}	Differential Figure 6	2.5	4.0	8.0	V/ns
High Level Output Voltage	V_{IH}	Differential	150			mV
Low Level Output Voltage	V_{IL}	Differential			-150	mV
Output Cross Point Voltage	V_{cross}	Figure 4	250		550	mV
Output Cross Point Voltage Deviation	V_{cross_delta}	Figure 5			140	mV
Output Ring Back Voltage Margin	V_{rb}	Figure 9	-100		100	mV
Output Ring Back Time	T_{stable}	Figure 10	500			ps
Average Clock Period Accuracy	T_{period_avg}		-300		2800	ppm
Absolute Period	T_{period_abs}	Figure 8	9.847		10.203	ns
Maximum Output Voltage	V_{max}	Single End Figure 4			1.15	V
Minimum Output Voltage	V_{min}	Single End Figure 4	-0.3			V
Output Duty Cycle	T_{outdc}	Figure 8	45	50	55	%
Time Matching of Output Rising and Falling	T_{slew_delta}	Figure 7			20	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
PCI Express Gen2 RMS Jitter	Jit_{RMS}	BW= 10kHz - 1.5MHz (2)		0.5	2.6	ps
		BW= 1.5MHz - 50MHz (2)		1.2	2.6	ps
Cycle to Cycle Jitter (p-p)	Jit_{c2c}	(3)		60	125	ps
Output Lock Time	T_{lock}	SS Off (4)		0.5	2	ms

Note:

(1) Specification of Frequency Accuracy is measured by connecting the standard 25MHz crystal unit for part number XRCGB25M000F3M00R0 of Murata Manufacturing Co., Ltd. on page 11.
This Output Clock Frequency Accuracy does not include accuracy of crystal unit.
Total output clock frequency accuracy could be up to “Output Clock Frequency Accuracy” + “Crystal unit accuracy”.

(2) The specifications are values applied the jitter filter function specified PCI Express standard.

(3) ±7σ in 10000 sampling or more

(4) Transition time to settle output into ±0.1% of specified frequency after escaping power down mode. (PCIE0_OE pin = PCIE1_OE pin = ‘L’).

Differential Output Measurement Circuit

Each Characteristic is measured at the point of "Measure point" in Figure 3

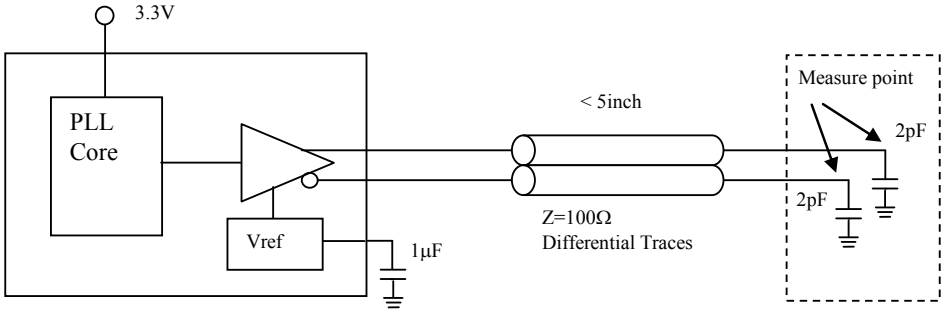


Figure 3. Differential Output Measurement Circuit

Definition of Differential Output AC Characteristics

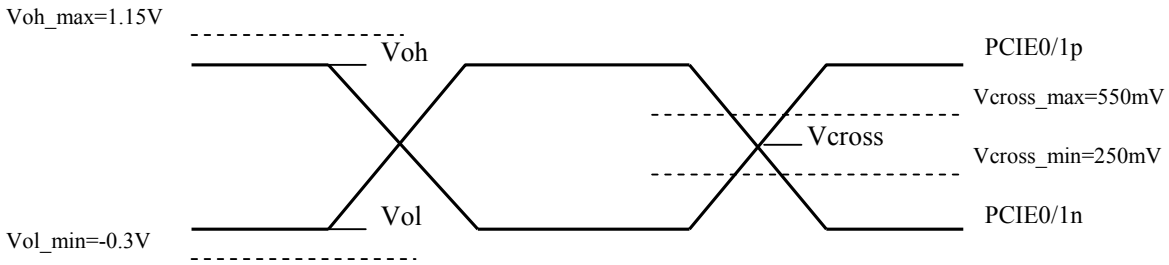


Figure 4. Definition of High / Low Level Voltage, Output Cross Point Voltage

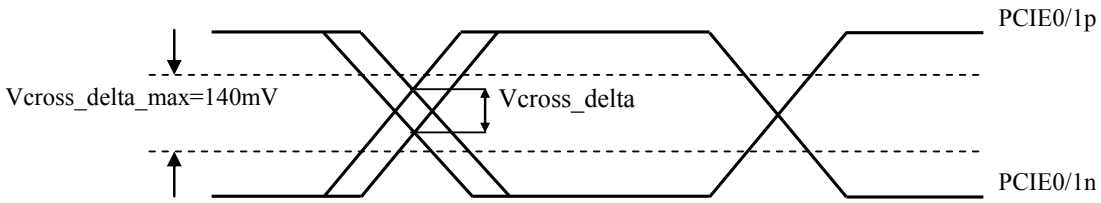


Figure 5. Definition of Output Cross Point Voltage Deviation

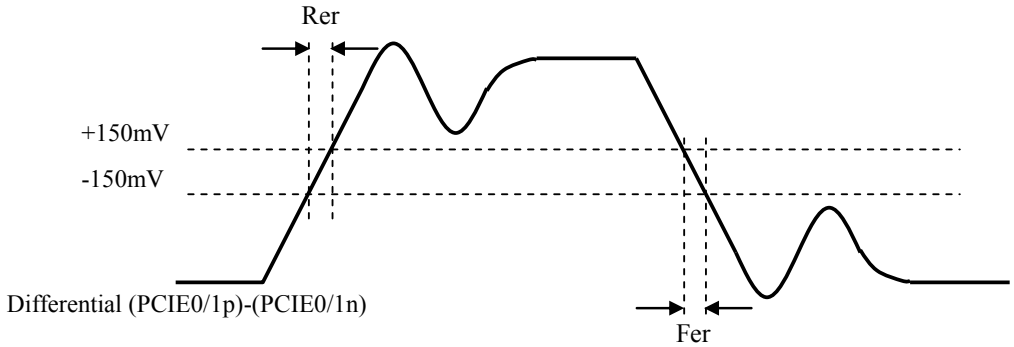
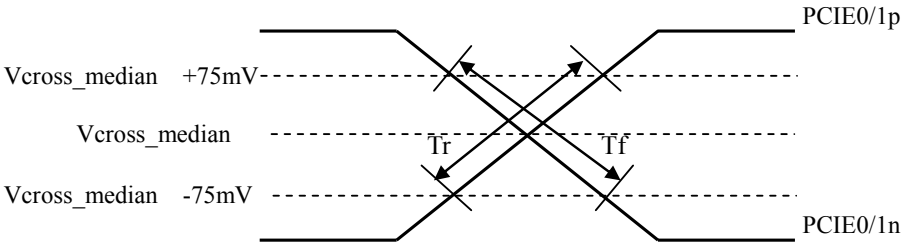
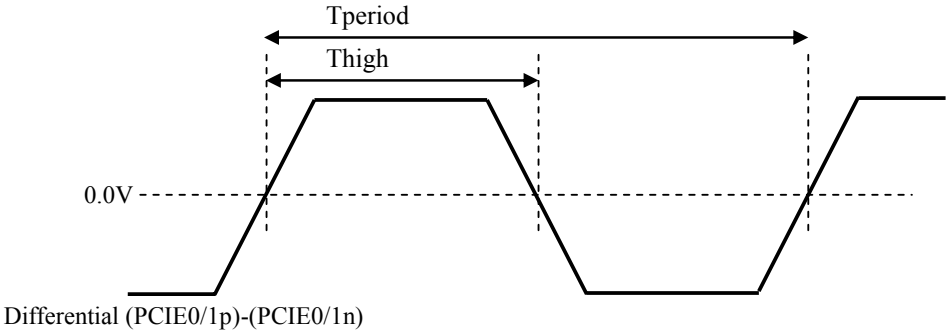


Figure 6. Definition of Output Slew Rate



T_{slew_delta} (%) = 100 * 2 * (Tr - Tf) / (Tr + Tf)

Figure 7. Definition of Time Matching of Output Rising and Falling



T_{outdc} (%) = 100 * Thigh / Tperiod

Figure 8. Definition of Output Duty Cycle

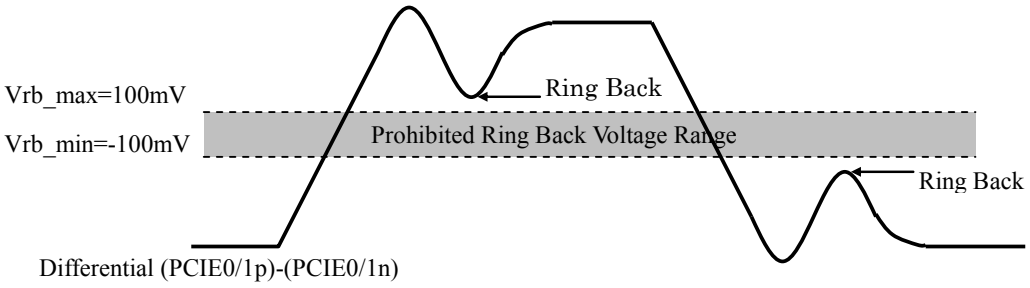


Figure 9. Definition of Output Ring Back Voltage Margin

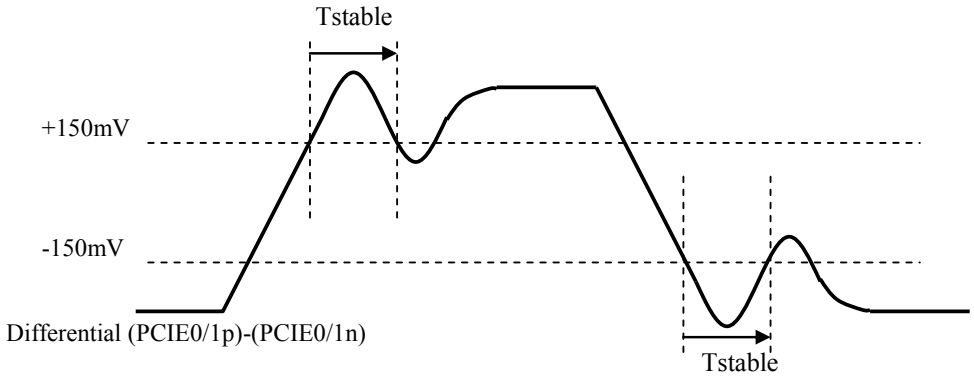


Figure 10. Definition of Output Ring Back Time

Crystal Specification

Murata Manufacturing Co.,Ltd, XRCGB25M000F3M00R0

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Crystal Clock Frequency	f0	CL=6[pF]		25.000		MHz
Series Resistance	R1			56.9	150	Ω
Shunt Capacitance	C0			0.59		pF
Motional Capacitance	C1			1.29		fF
Motional Inductance	L1			31.52		mH
Power level					300	μW

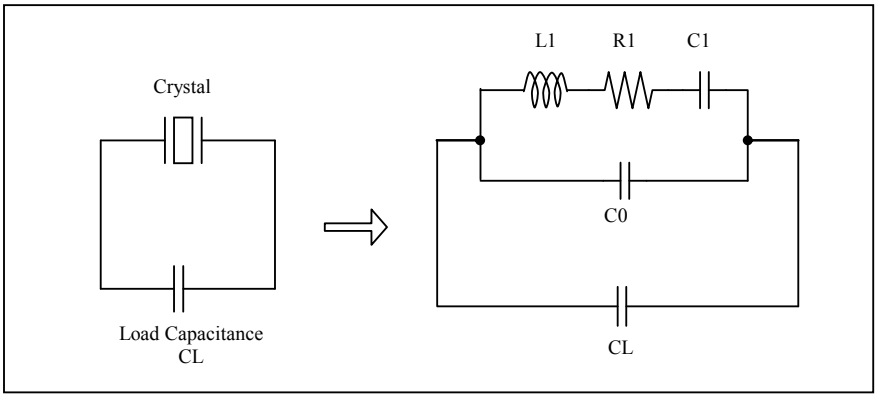


Figure 11. Equivalent parameters of crystal and load capacitance

9. Recommended External Circuits

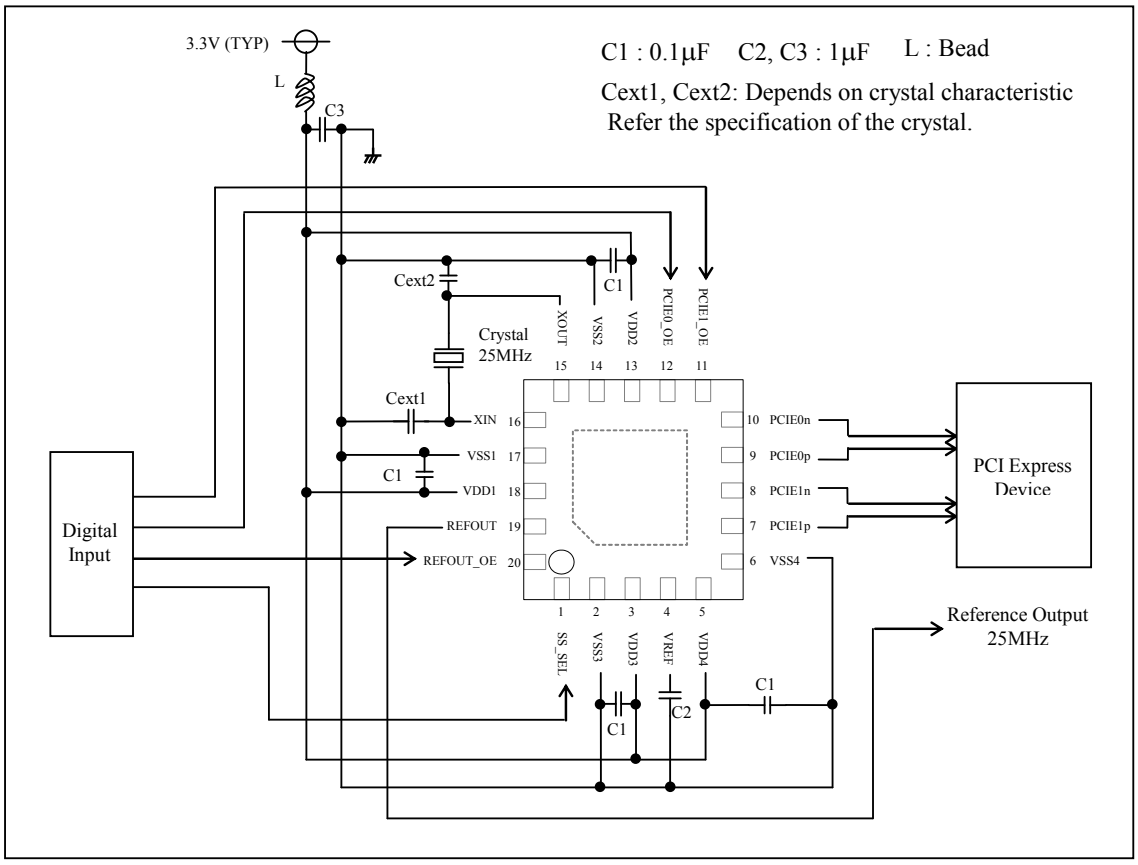


Figure 12 Recommended External Circuits

PCB Layout Consideration

The AK8160B2 is a high-accuracy and low-jitter clock generator. For proper performances specified in this datasheet, careful PCB layout should be taken. The followings are layout guidelines based on the typical connection diagram shown in Figure 12

Power supply line & Ground pin connection

AK8160B2 has four power supply pins (VDD1-4) which deliver power to internal circuitry segments.
And AK8160B2 has four ground pins (VSS1-4). These pins require connecting to plane ground which will eliminate any common impedance with other critical switching signal return.
0.1µF decoupling capacitors placed at VDD1, VDD2, VDD3 and VDD4 should be grounded at close to the VSS1pin, the VSS2 pin, VSS3 pin and the VSS4 pin, respectively.

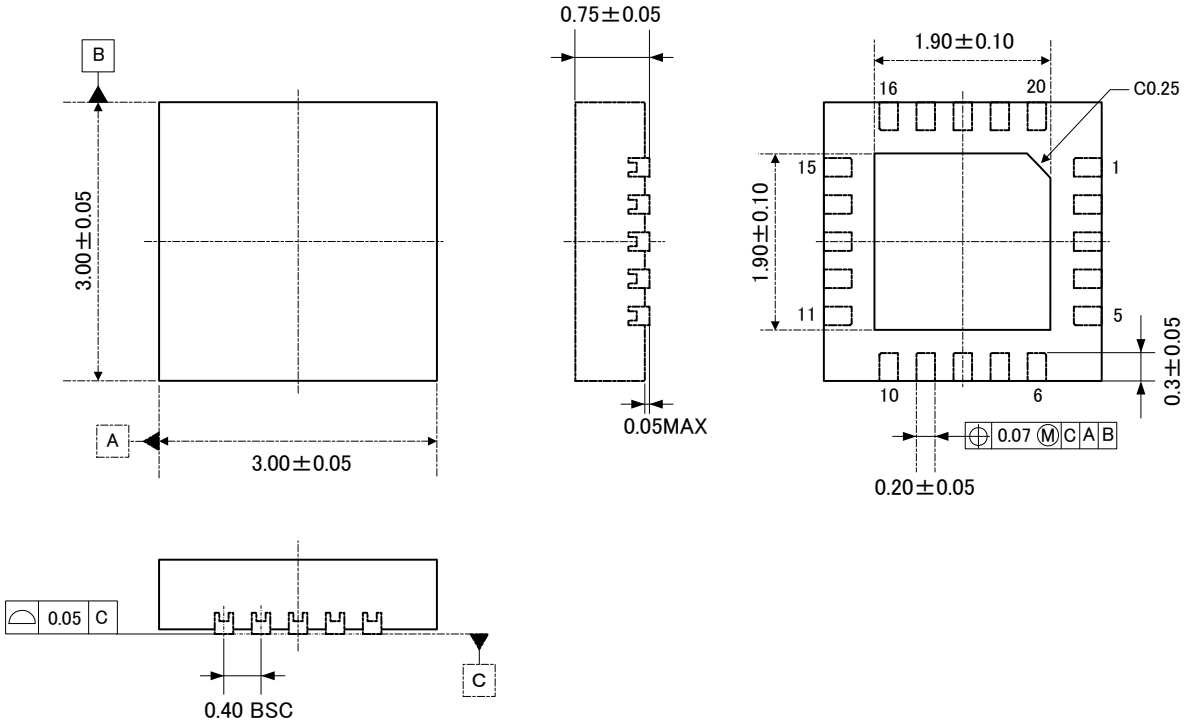
Crystal connection

Proper oscillation performance are susceptible to stray or parasitic capacitors around crystal. The wiring traces to a crystal form XIN (Pin 16) and XOUT (Pin 15) have equal lengths with no via and as short in length as possible. These traces should be also located away from any traces with switching signal.

10. Package

Outline Dimensions

0.4mm pitch 3mm x 3mm 20-pin QFN (Unit: mm)

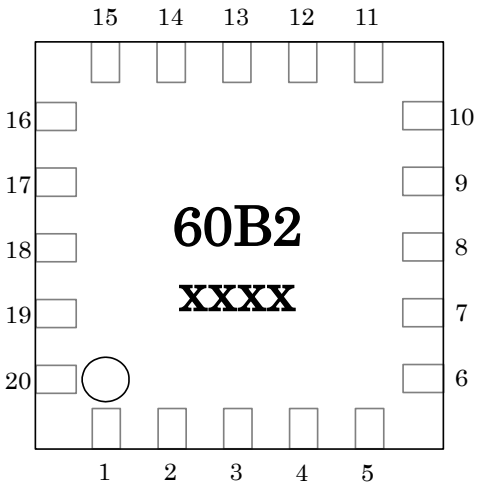


Package & Lead Frame Material

Package molding compound : Epoxy Resin (Green Compound)
Lead frame material : Cu Alloy
Lead frame surface treatment : Au

Marking

a: #1 Pin Index : Circle
b: Part number : 60B2
c: Date code : 4 digits



Revision History

Date	Revision	Reason	Page/Line	Contents
14/06/27	00	Initial Release.		

11. Important Notice

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