ISD8102 / ISD8104

2W Class AB Audio Amplifier

with Chip Enable

i) ISD8102 - Earphone Sense IN (SE / Diff)

ii) ISD8104 - Differential Input pair

1 GENERAL DESCRIPTION

The ISD8102/ ISD8104 are a general purpose analog audio amplifier, capable of driving a 4Ω load with up to 2Wrms output power. This device includes output current limiting, chip enable, low standby current and excellent pop-and-click suppression.

Also included is the ability to configure the input as either single-ended or differential. Internal resistors set the device to have default 20dB gain (ISD8102/ISD8104), and with external resistors any gain less than this can be achieved. The device is unity gain stable, including use with external feedback resistors and external capacitors as may be optionally used for implementing simple filtering functions.

ISD8102:

The ISD8102 output can be configured to drive either single ended or bridge tied loads (BTL). The Mode pin controls which configuration is active. This function is useful when using the IDS8102 to alternate between driving a speaker or a mono earpiece which is connected through a shorting phone jack. The Mode pin is connected to the normally closed pin of the shorting phone jack (see figure 3.1). When nothing is plugged into the jack, the external resistor holds the Mode pin low, enabling BTL mode. When a plug is inserted, the switch is opened and the mode pin goes to 1/2 VDD, as controlled by the resistor divider, putting the amplifier into single ended mode. Note that in this example, the speaker remains connected in both cases.

ISD8104:

The ISD8104 has differential inputs and can be configured to accept either single ended or differential signals.

2 FEATURES

- Wide power supply range and excellent standby current
  - o 2.0Vdc - 6.8Vdc operation
  - o <1uA standby current
- High output power (capless BTL configuration)
  - o Up to 2W output into 4Ω load (<10% distortion) with 6.8Vdc supply voltage
  - o < 0.1% distortion at 600mW into 8-ohms with 5Vdc supply voltage
- Excellent pop-and-click performance
  - o Low to inaudible pop/click using Chip Enable
- Single-Ended or Differential signal inputs
  - o > 75dB common mode rejection in differential mode
  - o > 70dB power supply noise rejection
- Very fast start-up time
  - o Less than 1msec when using Chip Enable
- Current limiting for over-current conditions
- Package options: Pb-free SOP-8, SOP-8 (Ex-Pad)
- Less BOM cost / Easy PCB layout
- Temperature Range: -40°C to +85°C

Applications:

- Toys
- Feature Phones
- Portable Game Consoles
- GPS
- Portable Speakers
- Boom Box
- White Goods

3 BLOCK DIAGRAM

3.1 ISD8102 WITH EARPIECE SENSE INPUT(PIN 3 = SE / BTL MODE)

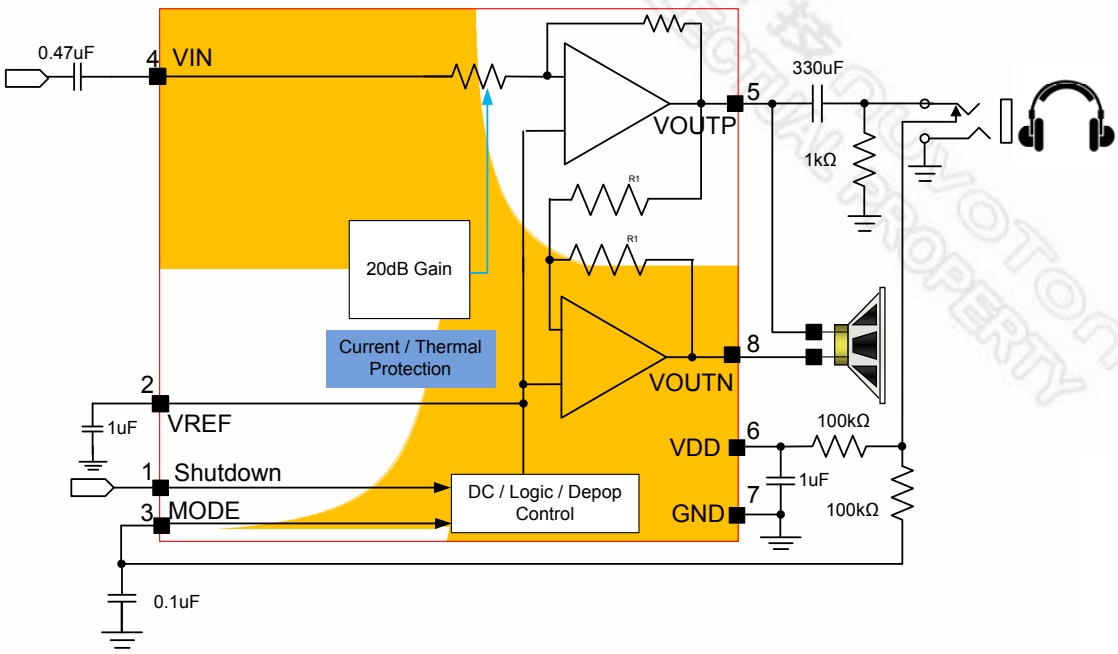


Figure 3-1 ISD8102 Earpiece Configuration Block Diagram

3.2 ISD8104 WITH DIFFERENTIAL INPUTS

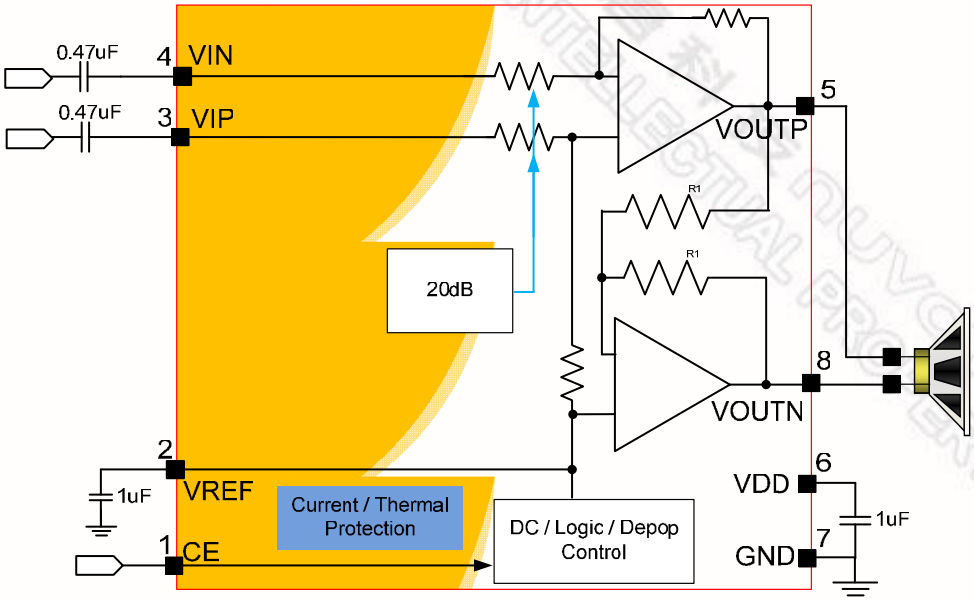


Figure 3-2 ISD8104 Differential Input Pair Block Diagram

4 PINOUT CONFIGURATION: SOP- 8

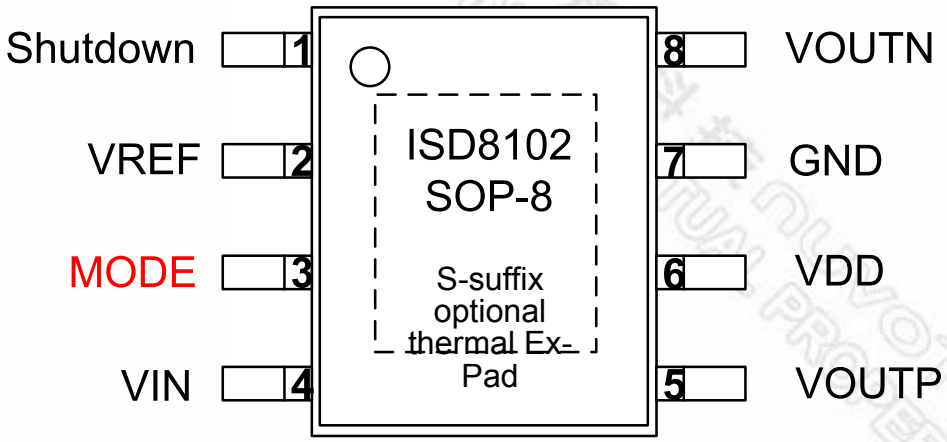


Figure 4-1 ISD8102 8-Lead SOP Pin Configuration

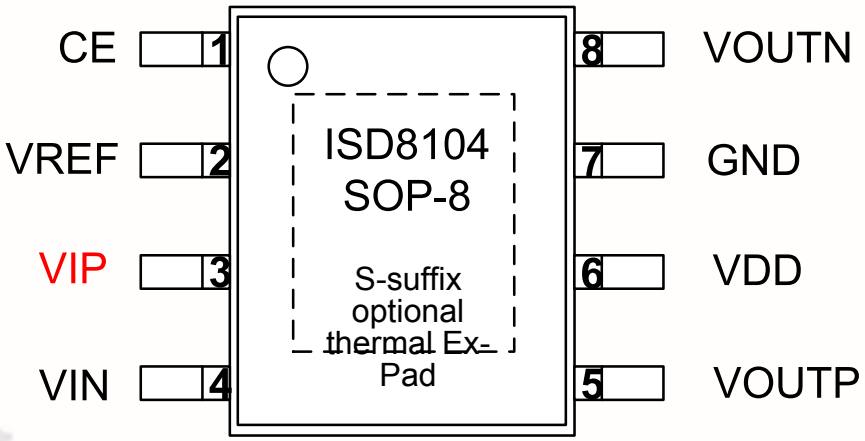


Figure 4-2 ISD8104 8-Lead SOP Pin Configuration

5 PIN DESCRIPTION

Pin Number	Pin Name	I/O	Function
1	Shutdown	I	Shutdown (Low = Chip Power Up / High = Chip Power Down)
2	VREF	O	Internal Reference Voltage (1/2 Vdd)
3	MODE	I	Single-Ended / Differential Output Logic Control
4	VIN	I	Inverting Signal Input
5	VOUTP	O	Non-Inverting Speaker Output
6	VDD	I	Supply Voltage
7	GND	I	Ground
8	VOUTN	O	Inverting Speaker Output
9	Ex-Pad	I	Thermal Tab (must be connected to Vss, SOP-8 package, only)

Table 5-1 ISD8102 8-Lead SOP Pin Description

Pin Number	Pin Name	I/O	Function
1	CE	I	Chip Enable
2	VREF	O	Internal Reference Voltage (1/2 Vdd)
3	VIP	I	Non-Inverting Signal Input
4	VIN	I	Inverting Signal Input
5	VOUTP	O	Non-Inverting Speaker Output
6	VDD	I	Supply Voltage
7	GND	I	Ground
8	VOUTN	O	Inverting Speaker Output
9	Ex-Pad	I	Thermal Tab (must be connected to Vss, SOP-8 package, only)

Table 5-2 ISD8104 8-Lead SOP Pin Description

6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (DIE)

CONDITIONS	VALUES
Operating temperature range [1]	-40°C to +85°C
Supply voltage (V_{DD})	+2.0V to +6.8V
Ground voltage (V_{SS})	0V
Input voltage (V_{DD})	Vss to V_{DD}
Voltage applied to any pins	(V_{SS} – 0.3V) to (V_{DD} + 0.3V)

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

CONDITIONS	VALUES
Operating temperature range (Case temperature) [1]	-40°C to +85°C
Supply voltage (V_{DD})	+2.0V to +6.8V
Ground voltage (V_{SS})	0V
Input voltage (V_{DD})	Vss to V_{DD}
Voltage applied to any pins	(V_{SS} – 0.3V) to (V_{DD} + 0.3V)

Notes: [1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.2 DC PARAMETERS

PARAMETER	SYMBOL	MIN	TYP [1]	MAX	UNITS	CONDITIONS
Supply Voltage	V_{DD}	2.0		6.8	V	
Operating Current	I_{DD}		2.6		mA	V_{DD}= 5V, no load
Standby Current	I_{SB}		0.1	1	µA	V_{DD}= 5V
CE input resistance			20k		Ω	Internal pull-down @ 0dB
CE input current			120		µA	CE=2.3V, V_{DD}= 5V
CE threshold enabled	V_{ENL}		0.9		V	All supply voltages
CE threshold standby	V_{ENH}		1.5		V	All supply voltages
VREF Reference Voltage			V_{DD}/2		V	

Notes: [1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by appropriate thermal design of the system.

6.3 AC PARAMETERS

6.3.1 Analog Characteristics; Cref = 1uF / Cvdd = 1uF

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Input Voltage Range			0.3 - 6.5		V	Vdd = 6.8Vdc
			0.3 – 3.4		V	Vdd = 3.7Vdc
			0.3 - 1.7		V	Vdd = 2.0Vdc
Inverting Input Impedance			TBD			Gain = 20dB
Non-Inverting Input Impedance			TBD			Gain = 20dB
Power Supply Rejection Ratio	PSRR		75		dB	Vdd = 5Vdc
Common Mode Rejection Ratio	CMRR		70		dB	Signal at INP = INV
Voltage Gain			20		dB	Rinput = 0 Ω
Enable Time from Standby			0.5		msec	Single-ended
Enable Time from Standby			0.5		msec	Differential
Pop-and-Click from Standby [1]			10		mV	Single Ended
Pop-and-Click from Standby [1]			10		mV	Differential
Thermal Resistance			60		°C/W	SOP-8 (with Ex-Pad)
Thermal Resistance			150		°C/W	SOP-8

Notes: [1] Impulse voltage that is potentially audible. After impulse, there is a slow ramp from standby Vref to operating Vref, which is typically inaudible with Cref = 1uF

6.3.2 Speaker Outputs

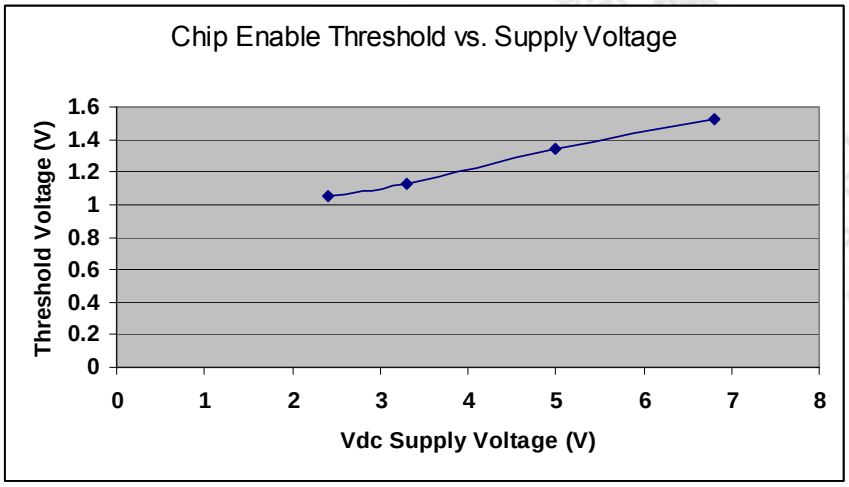
PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS
Signal-to-Noise Ratio	SNR		100		dB	0dB gain, 5Vdc
Load Impedance	$R_{L(SPK)}$		4		Ω	
Output Offset Voltage			8		mV	

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	UNITS	CONDITIONS (THD+N)
Output Power (BTL mode)	P_{BTL}		600		mW	<0.1% distortion
Load 4Ω	P_{BTL}		1600		mW	<1% distortion
Vdd=5Vdc / 0dB gain	P_{BTL}		2000		mW	<10% distortion

PARAMETER	SYMBOL	MIN	TYP[1]	MAX	Units	Conditions (THD+N)
Output Power (BTL mode)	P_{BTL}		600		mW	<0.1% distortion
Load 8Ω	P_{BTL}		1200		mW	<1% distortion
Vdd=5Vdc / 0dB gain	P_{BTL}		1400		mW	<10% distortion

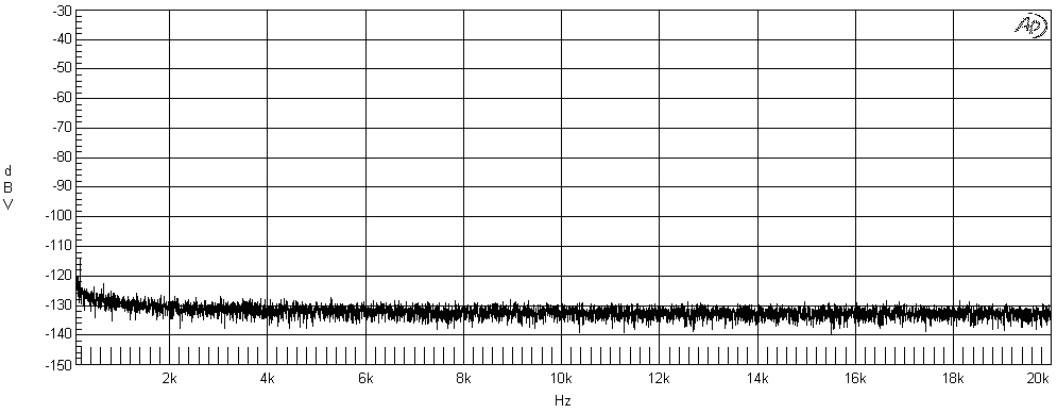
Notes: [1] Conditions V_{DD}=5V, T_A=25°C unless otherwise stated. Die temperature must at all times be kept less than 125°C by thermal design of the system.

6.3.3 Chip Enable Threshold Voltage

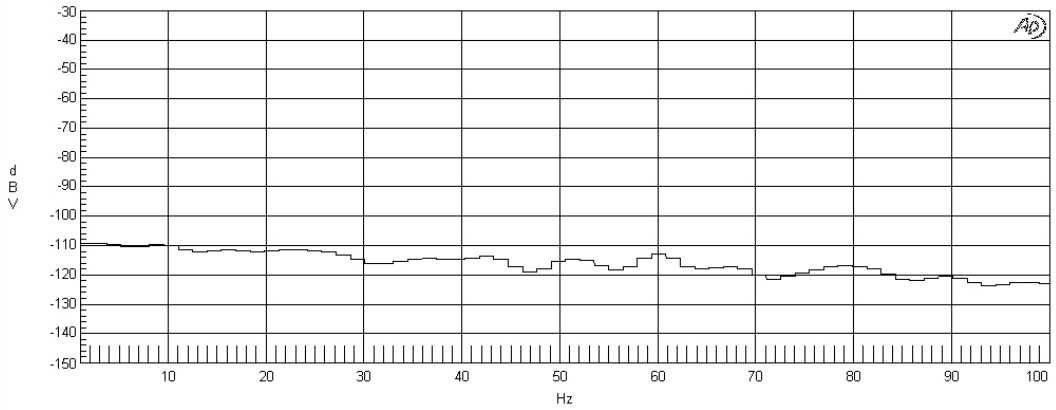


6.3.4 Output Noise Spectrum

Noise spectrum at Vdd = 5.0Vdc, Gain = 0dB, BW<22kHz

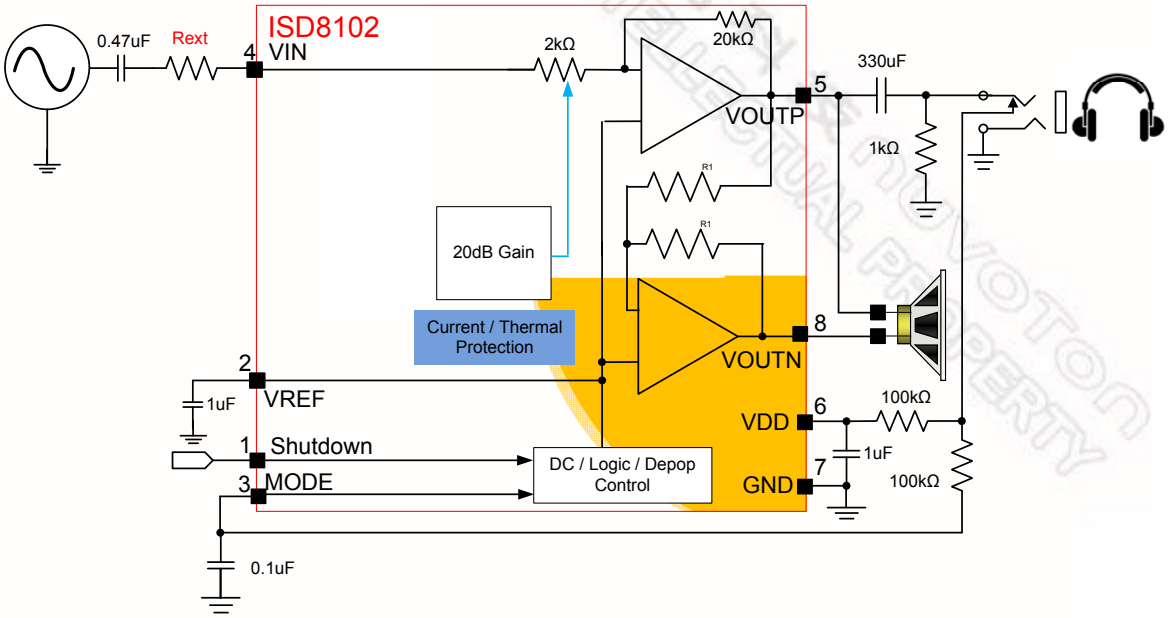


Noise Spectrum at Vdd = 5.0Vdc, Gain = 20dB, BW<22kHz



7 APPLICATION

7.1 GAIN SETTING – ISD8102



Differential Output Gain (VOUTP – VOUTN) =

$$2 \times \frac{20k\Omega}{2k\Omega + Rext}$$

By default: Rext = 0Ω,

ISD8102 Differential Output Gain = 20

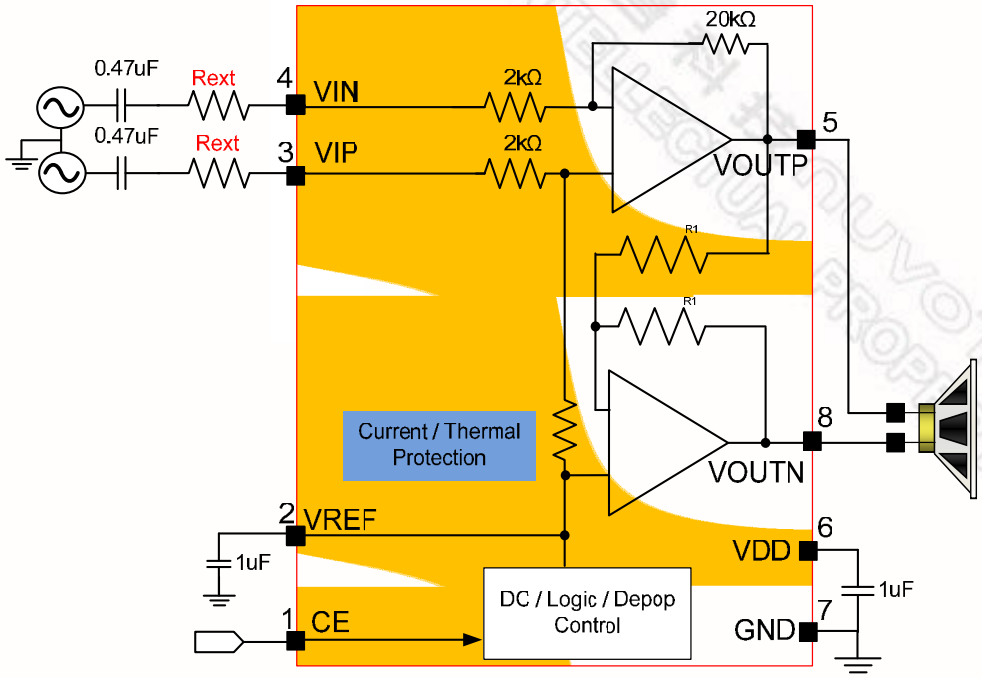
ISD8102 Differential Output Gain (in dB) = 20 x log (20) = 26dB

Example: Rext = 18kΩ

ISD8102 Differential Output Gain = 2

ISD8102 Differential Output Gain (in dB) = 20 x log (2) = 6dB

7.2 GAIN SETTING – ISD8104



Differential Output Gain (VOUTP – VOUTN) =

$$2 \times \frac{20k\Omega}{2k\Omega + Rext}$$

By default: Rext = 0Ω,

ISD8104 Differential Output Gain = 20

ISD8104 Differential Output Gain (in dB) = 20 x log (20) = 26dB

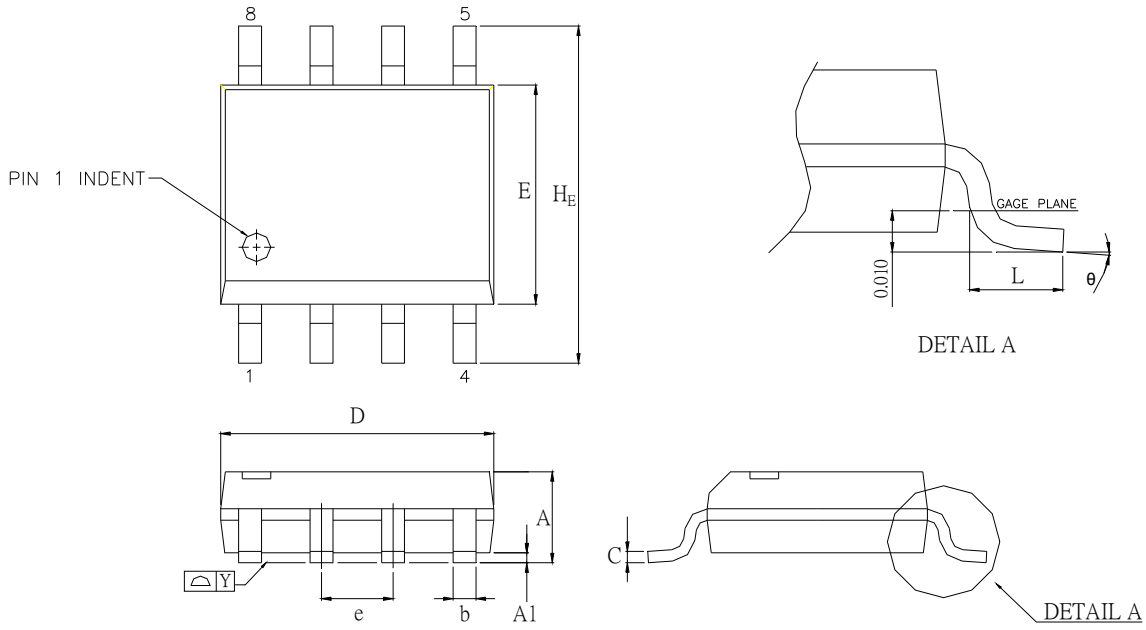
Example: Rext = 18kΩ

ISD8104 Differential Output Gain = 2

ISD8104 Differential Output Gain (in dB) = 20 x log (2) = 6dB

8 PACKAGE SPECIFICATION

8.1 SOP- 8

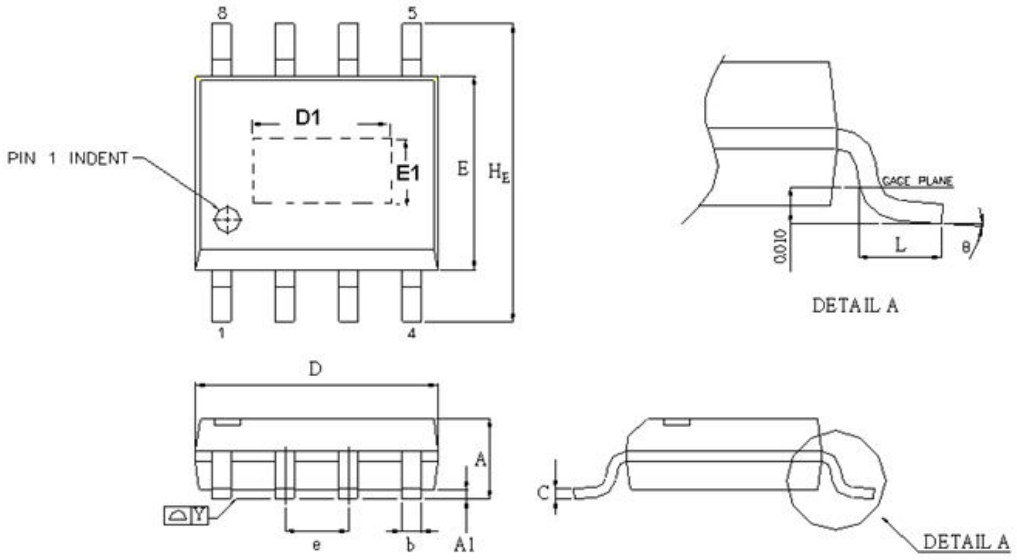


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	–	1.75	0.053	–	0.069
A1	0.05	–	0.15	0.002	–	0.006
b	0.33	–	0.51	0.013	–	0.020
C	0.19	–	0.25	0.008	–	0.010
D	4.8	–	5.00	0.188	–	0.196
E	3.8	–	4.0	0.150	–	0.157
e	1.27 BASIC			0.050 BASIC		
H_E	5.8	–	6.20	0.228	–	0.244
Y	–	–	0.10	–	–	0.004
L	0.40	–	1.27	0.016	–	0.050
θ	0°	–	10°	0°	–	10°

8.2 SOP- 8 (THERMAL EX-PAD)

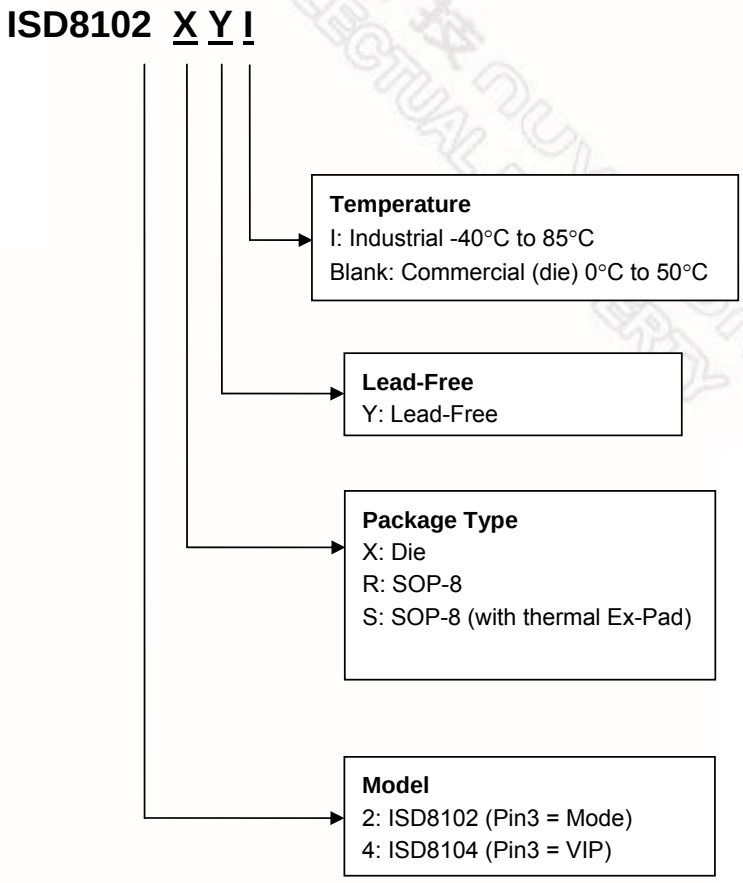
8L SOP-150mil (EX-PAD)



SYMBOLS	Dimensions In Millimeters		Dimensions In Inched	
	Min	Max	Min	Max
A	1.35	1.75	0.05	0.07
A1	0.05	0.25	0.00	0.01
b	0.31	0.51	0.01	0.02
c	0.10	0.25	0.00	0.01
D	4.70	5.10	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27 BASIC		0.05 BASIC	
H_E	5.80	6.20	0.23	0.24
Y	--	0.10	--	0.00
L	0.40	1.27	0.02	0.05
θ	0°	10°	0°	10°
D1	Depend on L/F size			
E1	Depend on L/F size			

D1-1	1.94	2.29	0.08	0.09
D1-2	2.81	3.30	0.11	0.13
D1-3	3.10	3.50	0.12	0.14
E1-1	1.94	2.29	0.08	0.09
E1-2	2.05	2.41	0.08	0.09
E1-3	2.20	2.60	0.09	0.10

9 ORDER INFORMATION



10 REVISION HISTORY

Version	Date	Description
0.0	Aug, 2010	Initial draft
1.0	Jun, 2011	Updated the specifications
1.1	Oct, 2011	Added the ISD8104 Gain Setting Calculation
1.2	Oct, 2011	Updated the specifications

Important Notice

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