



# AK4132

## 96kHz 24bit Sample Rate Converter

### 1. General Description

The AK4132 is an 2ch digital sample rate converter (SRC). It converts sample rate of the input audio source (from 8kHz to 96kHz) to 44.1kHz or 48kHz. The AK4132 has an internal oscillator and does not need any external master clocks. It contributes simplifying a system configuration. The AK4132 is suitable for the application interfacing to different sample rates such as Car Audio Systems and DVD recorders.

### 2. Features

- 2 channels Input/Output
- Asynchronous Sample Rate Converter
- Input Sample Rate Range (FSI): 8k ~ 96kHz
- Output Sample Rate (FSO): 44.1kHz, 48kHz
- Input to Output Sample Rate Ratio: FSO/FSI = 44.1/96 ~ 6
- THD+N: Up to -90dB
- Dynamic Range: 100dB (A-weighted, Typ.)
- I/F format: MSB justified, I<sup>2</sup>S compatible
- Oscillator for Internal Operation Clock
- Clock for Master mode: 256f<sub>so</sub>
- Power Supply: DVDD= 3.0 ~ 3.6V or 1.7 ~ 1.9V (LDO OFF Mode)
- Operating Temperature: -40 ~ +105°C
- Package: 16-pin TSSOP (0.65mm pitch)

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**4. Block Diagram**

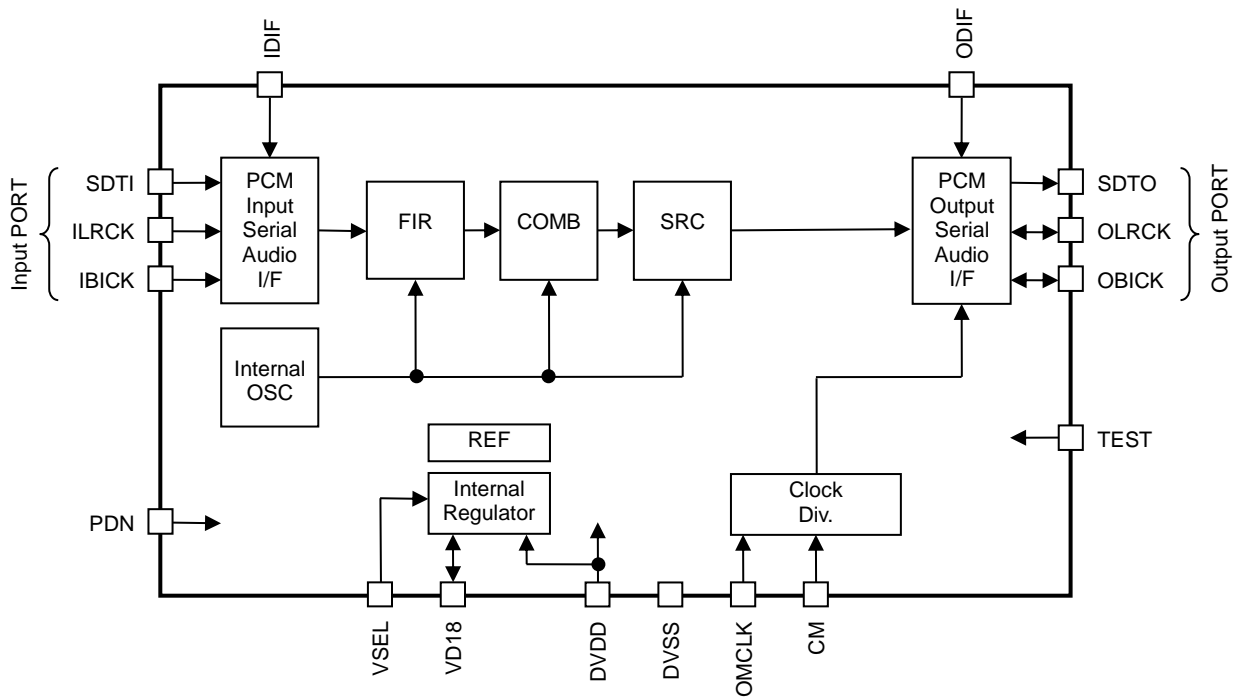


Figure 1. AK4132 Block Diagram

**5. Pin Configurations and Functions**

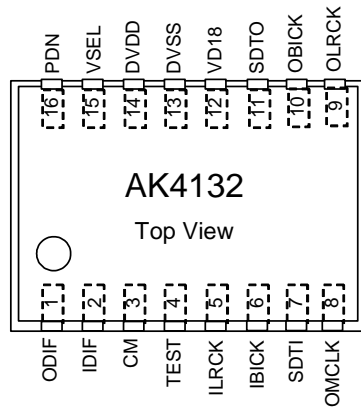


Figure 2. Pin Layout

## ■ Pin Functions

No.	Pin Name	I/O	Function	PDN= "L" Status
1	ODIF	I	Audio Interface Format Select Pin for Output PORT	-
2	IDIF	I	Audio Interface Format Select Pin for Input PORT	-
3	CM	I	Output Port Mode Select Pin "H": Slave Mode "L": Master Mode	-
4	TEST	I	Test pin. Must be connected to DVSS in normal use. It has a pull-down resistor 100kΩ.	-
5	ILRCK	I	Channel Clock Input Pin for Input PORT	-
6	IBICK	I	Audio Serial Clock Input Pin for Input PORT	-
7	SDTI	I	Audio Serial Data Input Pin for Input PORT	-
8	OMCLK	I	External Master Clock Input	-
9	OLRCK	O	Channel Clock Output Pin for Output PORT in Master Mode	"L"
		I	Channel Clock Input Pin for Output PORT in Slave Mode	-
10	OBICK	O	Audio Serial Clock Output Pin for Output PORT in Master Mode	"L"
		I	Audio Serial Clock Input Pin for Output PORT in Slave Mode	-
11	SDTO	O	Audio Serial Data Output Pin for Output PORT	"L"
12	VD18	I	Internal Digital Power Supply Pin, 1.7 ~ 1.9V (VSEL= "H")	-
		O	Regulator Output Pin, Typ. 1.8V (VSEL= "L") Current must not be taken from this pin. A 10μF (±30%; including the temperature characteristics) capacitor should be connected between this pin and DVSS. When this capacitor is polarized, the positive polarity pin should be connected to the VD18 pin.	"L"
13	DVSS	-	Digital Ground Pin	-
14	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V or 1.7 ~ 1.9V	-
15	VSEL	I	Internal Digital Power Supply Select Pin "H": External Power Supply "L": Internal Regulator	-
16	PDN	I	Power-Down Mode Pin "H": Power Up "L": Power Down and Reset The AK4132 should be reset once by bringing PDN pin = "L" upon power-up.	-

Note 1. All input pins should not be allowed to float.

Note 2. CM, ODIF and IDIF must be changed when the PDN pin = "L".

## ■ Handling of Unused Pin

Classification	Pin Name	Setting
Digital	OMCLK	Connect to DVSS

## 6. Absolute Maximum Ratings

(DVSS=0V; Note 3)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies	Digital	DVDD	-0.3	4.3	V
	Internal Digital	VD18	-0.3	2.5	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 4)		VDIN	-0.3	DVDD+0.3	V
Ambient Temperature (Power applied) (Note 5)		Ta	-40	105	°C
Storage Temperature		Tstg	-65	150	°C

Note 3. All voltages with respect to ground.

Note 4. ILRCK, IBICK, SDTI, IDIF, PDN, TEST, OMCLK, CM, ODIF, OBICK (Slave Mode), OLRCK (Slave Mode), VSEL pin

Note 5. PCB drawing density should be 100% or more.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.  
Normal operation is not guaranteed at these extremes.

## 7. Recommended Operating Conditions

(DVSS=0V; Note 3; VSEL= "L")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies	Digital	DVDD	3.0	3.3	3.6	V

Note 3. All voltages with respect to ground.

(DVSS=0V; Note 3; VSEL= "H")

Parameter		Symbol	Min.	Typ.	Max.	Unit
Power Supplies (Note 6)	Digital	DVDD	1.7	1.8	1.9	V
	Internal Digital	VD18	1.7	1.8	1.9	V
	Difference	DVDD-VD18		0		V

Note 3. All voltages with respect to ground.

Note 6. DVDD and VD18 must be connected externally.

\* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

<b>8. SRC Characteristics</b>
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(Ta= -40 ~ 105°C; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7V ~ 1.9V at VSEL pin= "H"; DVSS= 0V; Signal Frequency= 1kHz; measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input Sample Rate	FSI	8		96	kHz
Output Sample Rate	FSO	44.1		48	kHz
THD+N (Input= 1kHz, 0dBFS, <a href="#">Note 7</a> )					
FSO/FSI= 48kHz/48kHz		-	-101	-	dB
FSO/FSI= 48kHz/96kHz		-	-102	-	dB
FSO/FSI= 44.1kHz/96kHz		-	-101	-	dB
Worst Case (FSO/FSI=44.1kHz/32kHz)		-	-	-99	dB
Dynamic Range (Input= 1kHz, -60dBFS, <a href="#">Note 7</a> )					
FSO/FSI= 48kHz/48kHz		-	101	-	dB
FSO/FSI= 48kHz/96kHz		-	102	-	dB
FSO/FSI= 44.1kHz/96kHz		-	102	-	dB
Worst Case (FSO/FSI= 44.1kHz/32kHz)		101	-	-	dB
Dynamic Range (Input= 1kHz, -60dBFS, A-weighted, <a href="#">Note 7</a> )					
FSO/FSI= 48kHz/48kHz		-	104	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	44.1/96		6	-

Note 7. Measured by Audio Precision, System Two.

<b>9. Consumption Current</b>
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■ Internal Regulator (VSEL pin= "L")

(Ta= -40 ~ 105°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation:					
FSI=FSO= 48kHz at Master Mode :DVDD= 3.3V			6	-	mA
DVDD= 3.6V				8	mA
FSI= 96kHz, FSO= 48kHz at Master Mode :DVDD= 3.3V			10		mA
DVDD= 3.6V				12	mA
Power down: PDN = "L" (Note 8) DVDD=3.6V			10	100	μA

Note 8. All digital input pins including clock pins are connected to DVSS.

■ External VD18 (VSEL pin= "H")

(Ta= -40 ~ 105°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Current					
Normal operation:					
FSI=FSO=48kHz at Master Mode:					
DVDD=VD18=1.8V			6	-	mA
DVDD=VD18=1.9V				8	mA
FSI=96kHz, FSO=48kHz at Master Mode:					
DVDD=VD18=1.8V			10	-	mA
DVDD=VD18=1.9V				12	mA
Power down: PDN = "L" (Note 9) DVDD=VD18=1.9V			10	100	μA

Note 9. Except the VSEL pin, all digital input pins including clock pins are connected to DVSS.

<b>10. Filter Characteristics</b>
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■ **Short Delay Sharp Roll-Off Filter Characteristics**

( $T_a = -40 \sim 105^\circ\text{C}$ ;  $DVDD = 3.0 \sim 3.6\text{V}$  at  $V_{SEL}$  pin= "L" or  $DVDD = VD18 = 1.7 \sim 1.9\text{V}$  at  $V_{SEL}$  pin= "H";  $DVSS = 0\text{V}$ )

Parameter		Symbol	Min.	Typ.	Max.	Unit
<b>Digital Filter</b>						
Passband -0.01dB	$0.985 \leq FSO/FSI \leq 6.000$	PB	0		0.4583FSI	kHz
	$0.714 \leq FSO/FSI < 0.985$	PB	0		0.4167FSI	kHz
	$0.536 \leq FSO/FSI < 0.714$	PB	0		0.2182FSI	kHz
	$0.492 \leq FSO/FSI < 0.536$	PB	0		0.2177FSI	kHz
	$0.324 \leq FSO/FSI < 0.492$	PB	0		0.1948FSI	kHz
	$0.246 \leq FSO/FSI < 0.324$	PB	0		0.0917FSI	kHz
	$0.1667 \leq FSO/FSI < 0.246$	PB	0		0.0826FSI	kHz
Stopband	$0.985 \leq FSO/FSI \leq 6.000$	SB	0.5417FSI			kHz
	$0.714 \leq FSO/FSI < 0.985$	SB	0.5021FSI			kHz
	$0.536 \leq FSO/FSI < 0.714$	SB	0.2974FSI			kHz
	$0.492 \leq FSO/FSI < 0.536$	SB	0.2813FSI			kHz
	$0.324 \leq FSO/FSI < 0.492$	SB	0.2604FSI			kHz
	$0.246 \leq FSO/FSI < 0.324$	SB	0.1573FSI			kHz
	$0.1667 \leq FSO/FSI < 0.246$	SB	0.1471FSI			kHz
Passband Ripple	$0.1667 \leq FSO/FSI \leq 6.000$	PR			$\pm 0.01$	dB
Stopband Attenuation	$0.985 \leq FSO/FSI \leq 6.000$	SA	-92.8			dB
	$0.714 \leq FSO/FSI < 0.985$	SA	-93.5			dB
	$0.536 \leq FSO/FSI < 0.714$	SA	-94.5			dB
	$0.492 \leq FSO/FSI < 0.536$	SA	-92.9			dB
	$0.324 \leq FSO/FSI < 0.492$	SA	-92.0			dB
	$0.246 \leq FSO/FSI < 0.324$	SA	-94.4			dB
	$0.1667 \leq FSO/FSI < 0.246$	SA	-93.8			dB
Group Delay (Note 10)		GD	-	18	-	1/fs

Note 10. This value is the time from a rising edge of LRCK after L/R data is input to a rising edge of LRCK before the L/R data is output when there is no phase difference between the input and the output data.



<b>11. DC Characteristics</b>
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(Ta= -40 ~ 105°C; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= "H"; DVSS= 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage (Note 11)	VIH	70%DVDD	-	-	V
Low-Level Input Voltage (Note 11)	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout= -400μA) (Note 12)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= 400μA) (Note 12)	VOL	-	-	0.4	V
Input Leakage Current	(Note 11, Except TEST pin)	-10	-	10	μA
	TEST pin 100kΩ Pull down	-10		72	μA

Note 11. ILRCK, IBICK, SDTI, IDIF, PDN, TEST, OMCLK, CM, ODIF, OBICK (Slave Mode), OLRCK (Slave Mode) and VSEL pin.

Note 12. SDTO, OBICK (Master Mode) and OLRCK (Master Mode) pin

<b>12. Switching Characteristics</b>
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■ **Clock**

(Ta= -40 ~ 105°C; DVDD= 3.0 ~ 3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin= "H";  
C<sub>L</sub>= 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
<b>Master Clock Input (OMCLK)</b>					
256 FSO :					
Frequency	fCLK	11.2896		12.288	MHz
Pulse Width Low	tCLKL	40			ns
Pulse Width High	tCLKH	40			ns
<b>Channel Clock for Input Port (ILRCK)</b>					
Frequency					
Normal Speed Mode	FSIN	8		54	kHz
Double Speed Mode	FSID	54		108	kHz
Duty Cycle	dILRCK	48	50	52	%
<b>Channel Clock for Output Port (OLRCK)</b>					
<b>Slave Mode</b>					
Frequency	FSO	44.1		48	kHz
<b>Master Mode</b>					
Frequency					
OMCLK Input 256FSO Mode	FSO	44.1		48	kHz
Duty Cycle					
Slave Mode	dOLRCK	48	50	52	%
Master Mode	dOLRCK		50		%

### ■ Audio Interface Timing

(Ta= -40 ~ 105°C; DVDD= 3.0 ~3.6V at VSEL pin= "L" or DVDD= VD18= 1.7 ~ 1.9V at VSEL pin="H";  
C<sub>L</sub>= 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
<b>Audio Interface Timing</b>					
<b>Input PORT</b>					
IBICK Period Normal speed Mode	tIBCK	1/256 FSIN			ns
Double speed Mode	tIBCK	1/128 FSID			ns
IBICK Pulse Width Low	tIBCKL	27			ns
IBICK Pulse Width High	tIBCKH	27			ns
ILRCK Edge to IBICK "↑" (Note 13)	tILRB	15			ns
IBICK "↑" to ILRCK Edge (Note 13)	tIBLR	15			ns
SDTI Hold Time from IBICK "↑"	tISDH	15			ns
SDTI Setup Time to IBICK "↑"	tISDS	15			ns
<b>Output PORT (Slave Mode)</b>					
OBICK Period Normal speed Mode	tOBCK	1/256 FSO			ns
OBICK Pulse Width Low	tOBCKL	27			ns
OBICK Pulse Width High	tOBCKH	27			ns
OLRCK Edge to OBICK "↑" (Note 13)	tOLRB	20			ns
OBICK "↑" to OLRCK Edge (Note 13)	tOBLR	20			ns
OLRCK to SDTO(MSB) (Except I <sup>2</sup> S Mode)	tOLRS			20	ns
OBICK "↓" to SDTO	tOBSD			20	ns
<b>Output PORT (Master Mode)</b>					
OBICK Frequency	fOBCK		64 FSO		Hz
OBICK Duty	dOBCK		50		%
OBICK "↓" to OLRCK Edge	tOMBLR	-20		20	ns
OBICK "↓" to SDTO	tOBSD	-20		20	ns
<b>Reset Timing</b>					
PDN Pulse Width (Note 14)	tPD	150			ns
PDN pin Pulse Width of Spike Noise Suppressed by Input Filter (Note 15)	tPDS	0		50	ns

Note 13. BICK rising edge must not occur at the same time as LRCK edge.

Note 14. The AK4132 can be rest by bringing the PDN pin = "L".

Note 15. Spike noise width of "L" pulse suppressed by input filter of the PDN pin.

■ Timing Diagram

Master Clock

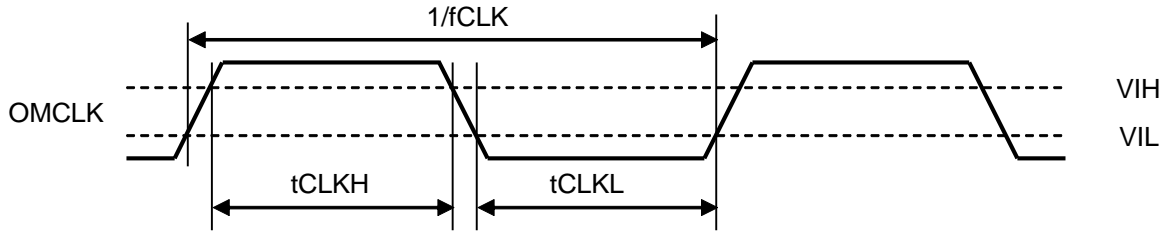


Figure 3. OMCLK Clock Timing

Input Port Clock

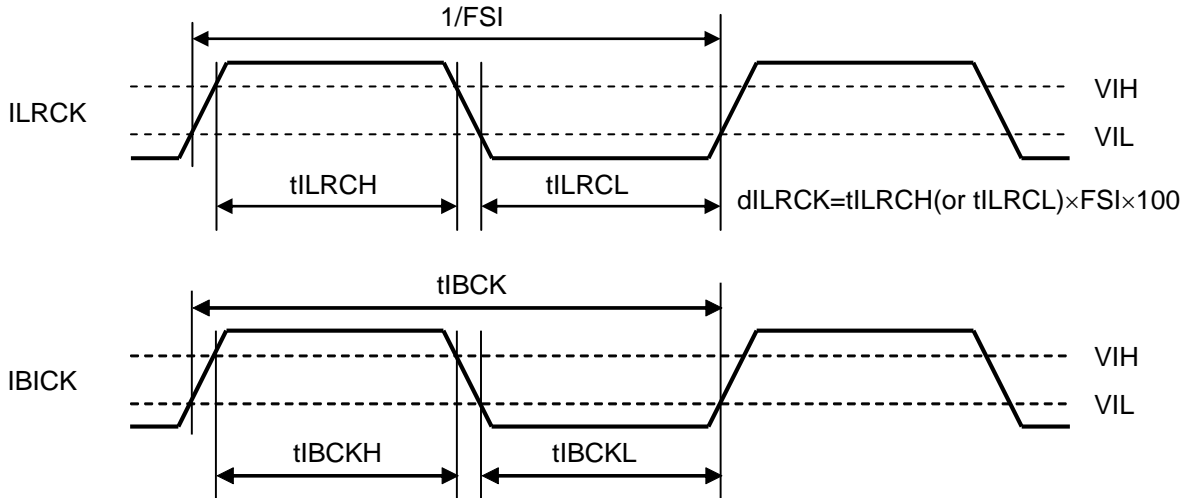


Figure 4. ILRCK, IBICK Clock Timing

Input Port Timing

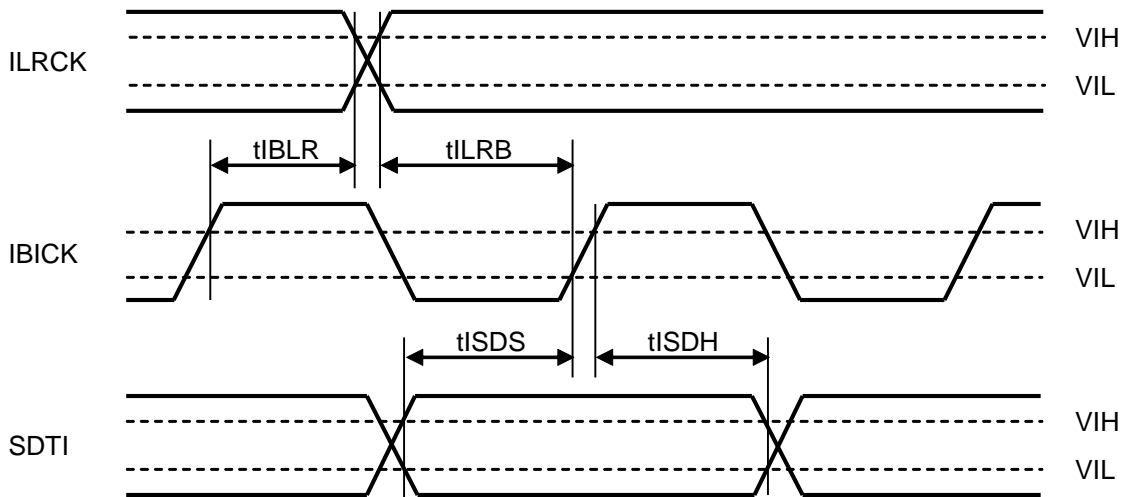


Figure 5. Input PORT Audio Interface Timing

**Output Port Clock (Slave Mode)**

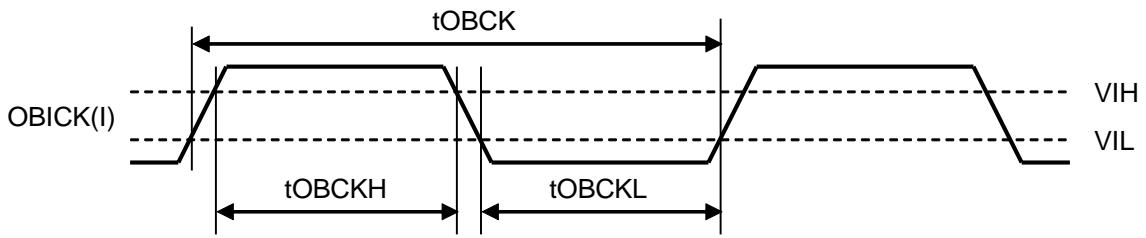
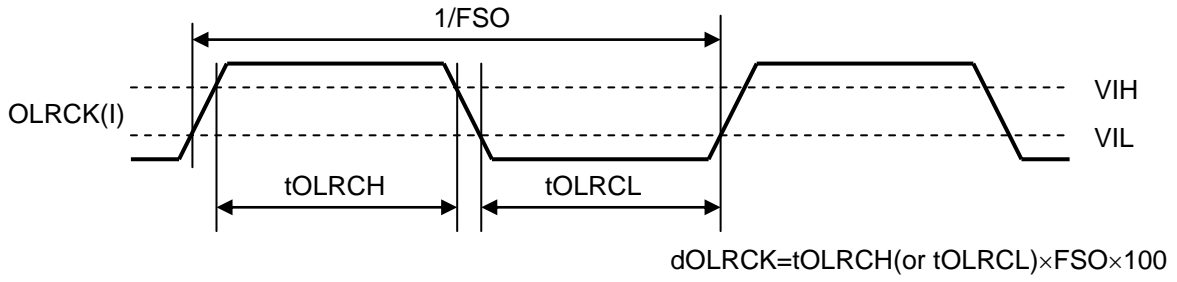


Figure 6. OLRCK, OBICK Clock Timing (Slave Mode)

**Output Port Timing (Slave Mode)**

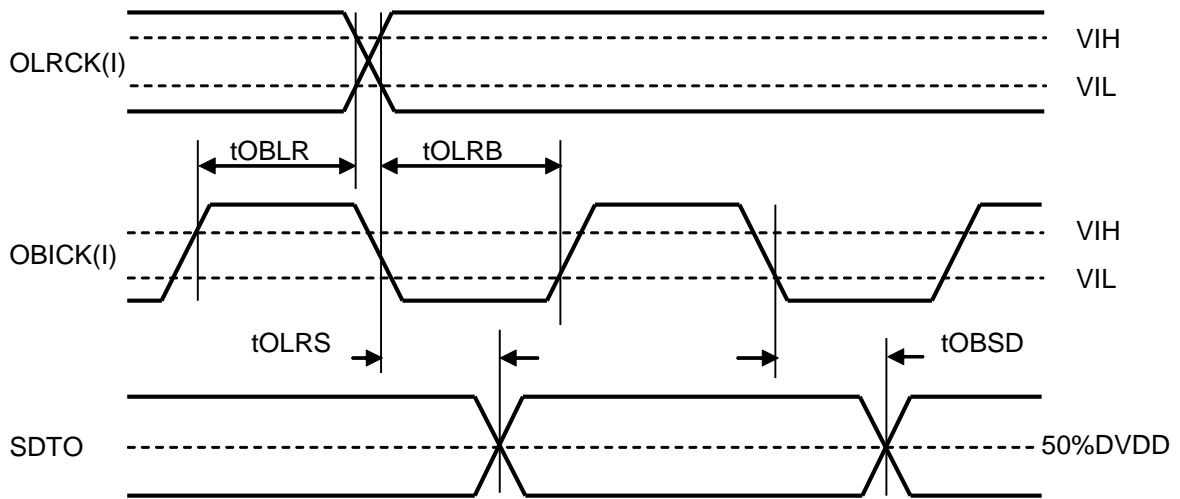


Figure 7. Output PORT Audio Interface Timing (Slave Mode)

**Output Port Clock (Master Mode)**

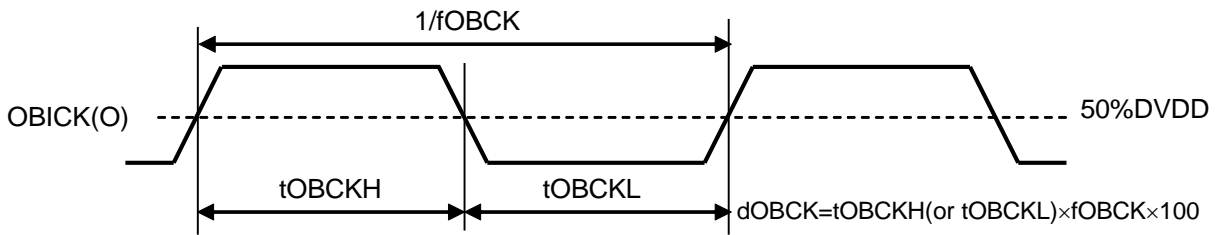
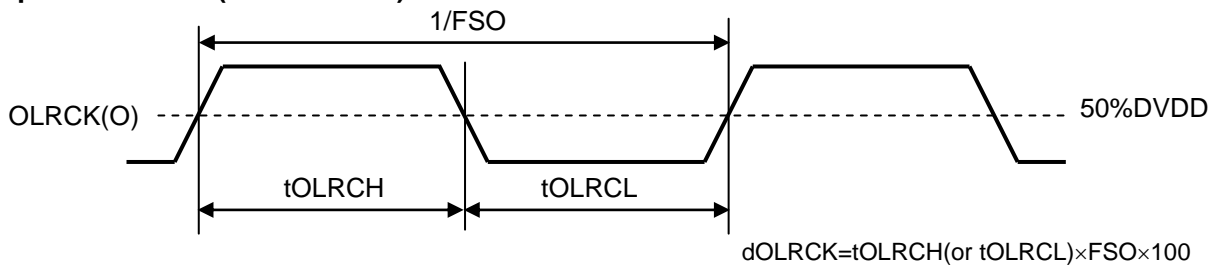


Figure 8. OLRCK, OBICK Clock Timing (Master Mode)

**Output Port Timing (Master Mode)**

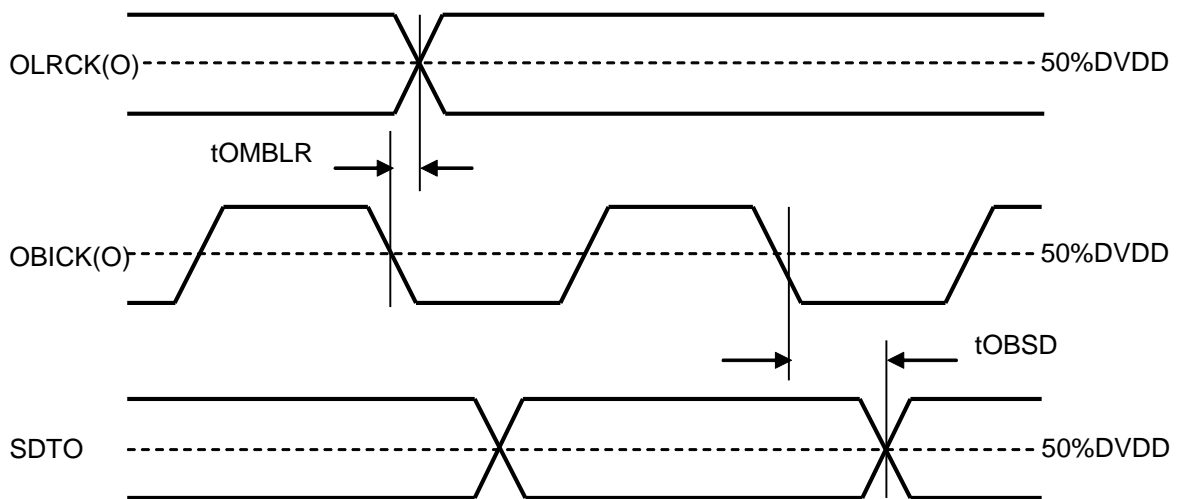


Figure 9. Output PORT Audio Interface Timing (Master Mode)

**Power-down Timing**

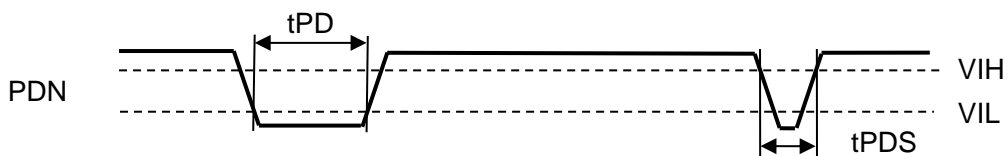


Figure 10. Power Down and Reset Pulse

### 13. Functional Description

#### ■ System Clock and Audio Interface Format for Input Port

The audio interface format is controlled by the IDIF pin. The data format is MSB first in 2's complement. The SDTI input data is clocked in on a rising edge of the IBICK. The audio interface format of the input port should be changed while the PDN pin = "L".

Table 1. Input PORT Audio Interface Format

Mode	IDIF Pin	SDTI Format	ILRCK	IBICK	IBICK Freq
0	L	24-bit, MSB justified	Input	Input	$256FSI \geq$ or $\geq 64FSI$
1	H	24 or 16-bit, I <sup>2</sup> S Compatible 16-bit, I <sup>2</sup> S Compatible			$256FSI \geq$ or $\geq 64FSI$ 32FSI (Note 16)

Note 16. When IBICK = 32FSI, only 16-bit I<sup>2</sup>S Compatible is supported.

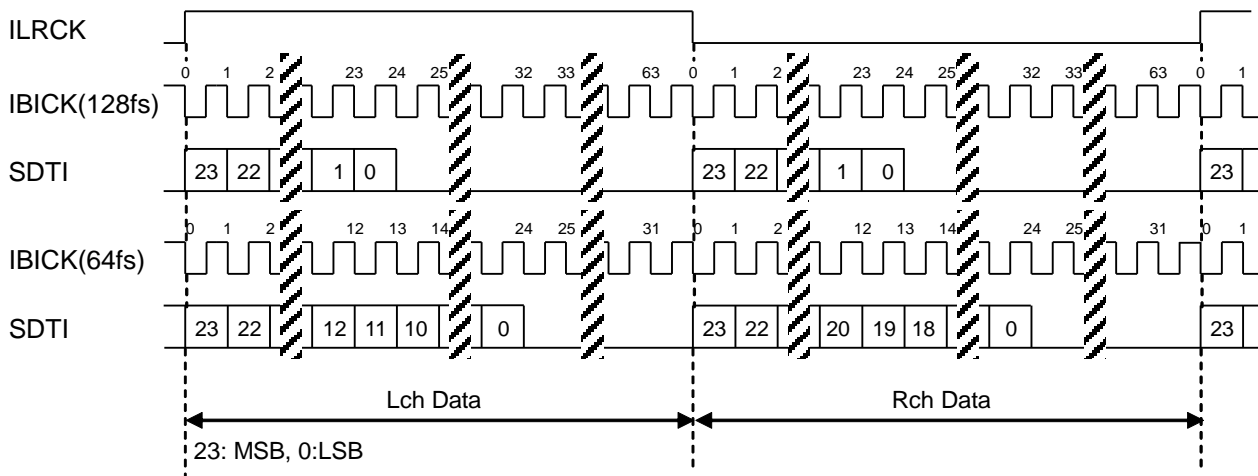


Figure 11. Mode0 Timing (24-bit MSB)

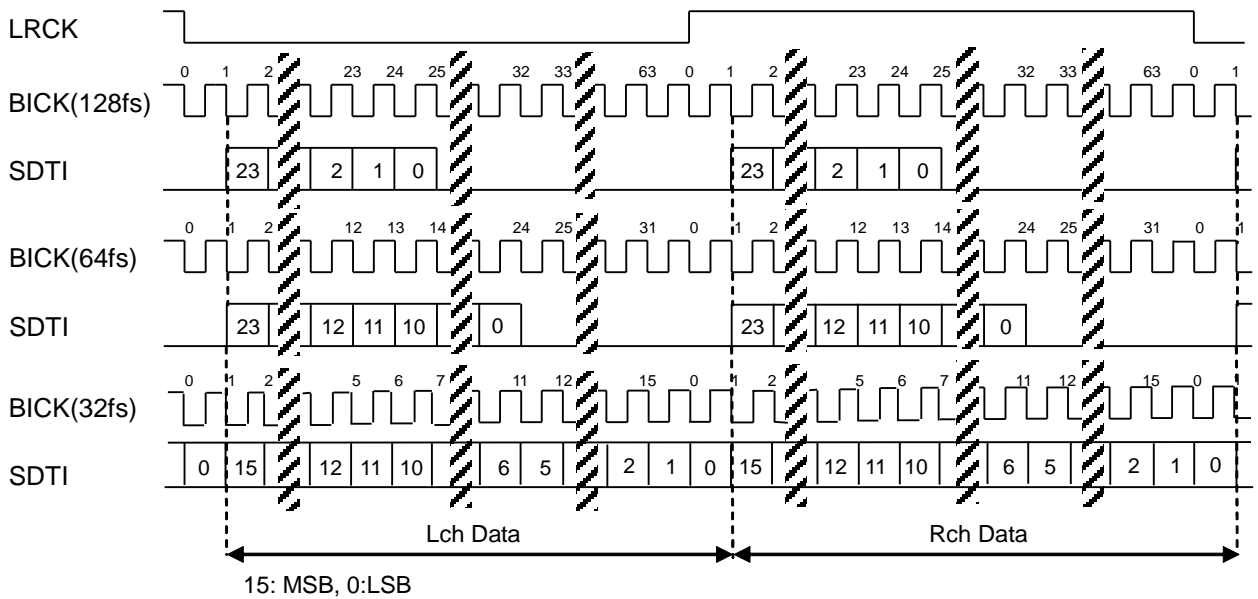


Figure 12. Mode1 Timing (24-bit/16-bit I<sup>2</sup>S)

■ System Clock for Output PORT

The output ports work in both master mode and slave mode. In master mode, the output port is operated with OLRCK and OBICK generated from OMCLK. OLRCK and OBICK clocks are output from the OLRCK pin and OBICK pin, respectively. In slave mode, the output port is operated by input clocks from the OLRCK pin and the OBICK pin. The OMCLK pin is not used in slave mode. It must be connected to DVSS.

The CM pin selects master or slave mode.

Table 2. Output PORT Master/Slave Mode Control

Mode	CM pin	Master / Slave	OMCLK Frequency	FSO
0	L	Master	256FSO	44.1kHz, 48kHz
1	H	Slave	Not used. (Note 17)	44.1kHz, 48kHz

Note 17. The OMCLK pin must be connected to DVSS in slave mode.

■ Audio Interface Format of the Output Port

The ODIF pin controls the audio interface mode of the output port. The data format is MSB first in 2's complement. The data is output on a falling edge of OBICK from the SDTO pin. The audio interface format of the output port should be changed while the PDN pin = "L".

Table 3. Output PORT Audio Interface Format

Mode	ODIF pin	SDTO Format	OBICK (Slave)	OBICK (Master)
0	L	MSB justified	≥ 48fs or 32fs	64fs
1	H	I <sup>2</sup> S Compatible	≥ 48fs or 32fs	64fs

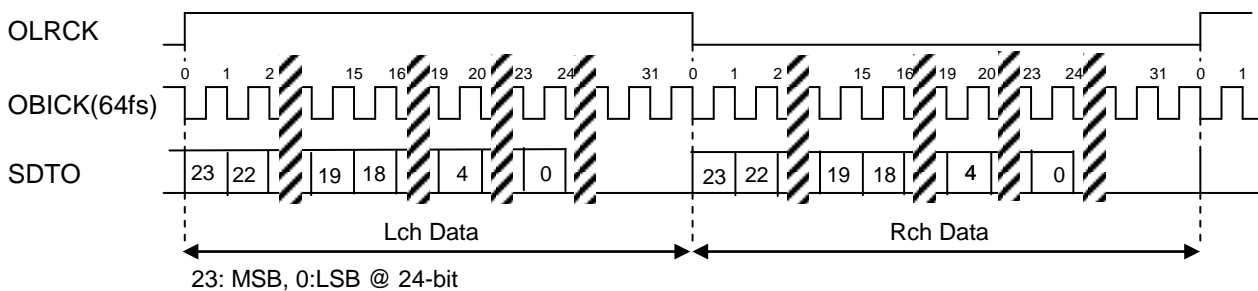


Figure 13. Mode 0 MSB Justified Timing

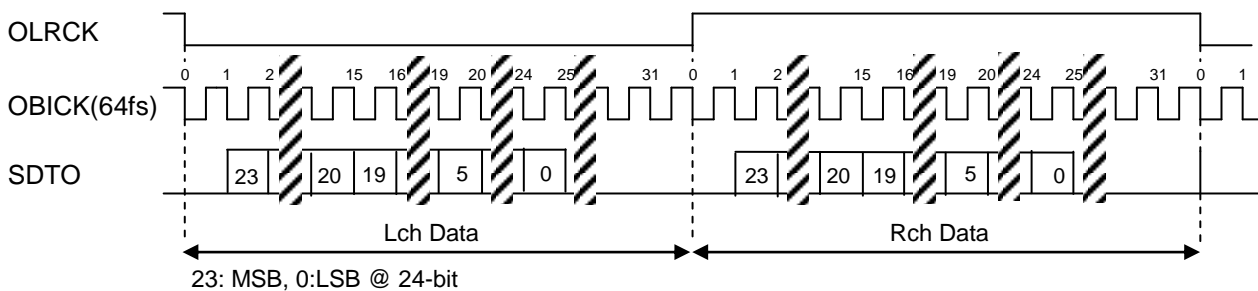


Figure 14. Mode 1 I<sup>2</sup>S Compatible Timing



■ Regulator

The AK4132 has an internal regulator which suppresses the voltage to 1.8V from DVDD (3.3V). The generated 1.8V power is used as power supply for internal circuit. When over-current is flowed to the regulator output, over-current detection circuit works. When over-voltage is flowed to the regulator output, over-voltage detection circuit works. The regulator block is powered-down and the AK4132 becomes reset state when over-current detection circuit or over-voltage detection circuit is operated. The AK4132 does not return to normal operation without a reset by the PDN pin when these detection circuits are worked. When over-current or over-voltage is detected, the PDN pin should be brought into “L” at once, and should be set to “H” again to recover normal operation.

■ Power Supply

The AK4132 supports both 1.8 V and 3.3 V power supplies. Set the VSEL pin according to the power supply voltage. When using a 3.3 V power, set the VSEL pin to “L”. The internal regulator is turned ON and starts generating a 1.8 V for internal circuits from a 3.3 V power supplied to the DVDD pin by the VSEL pin = “L”. When using a 1.8 V power, set the VSEL pin to “H”. The internal regulator is turned OFF and the VD18 pin will be a power supply pin for the internal circuits. In this case, supply a 1.8 V power to both the DVDD pin and the VD18 pin.

■ System Reset

Bringing the PDN pin = “L” sets the AK4132 power-down mode and initializes the digital filters. The AK4132 should be reset once by bringing the PDN pin to “L” upon power-up. The internal SRC circuit is powered-up on an edge of ILRCK and OLRCK after a power-up period of the internal regulator (PDN pin = “H”). The data output time of the SDTO pin depends on the ILRCK and OLRCK input when the PDN pin = “H” as Figure 15 and Figure 16.

Case 1: ILRCK and OLRCK are input when the PDN pin= “H”

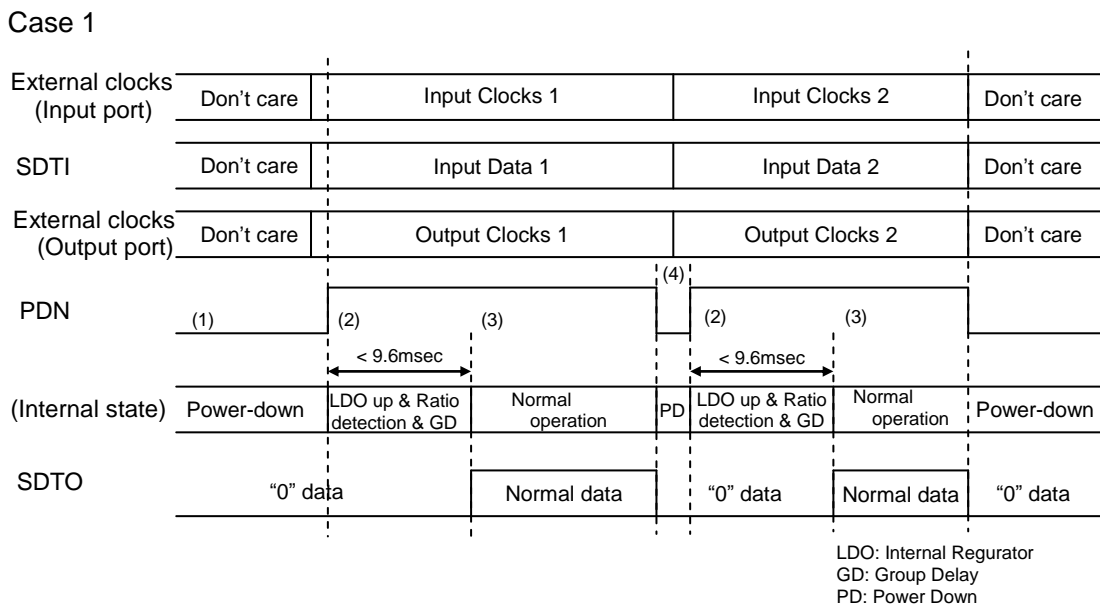


Figure 15. System Reset Case1

Notes:

- (1) The SDTO pin outputs “L” when the PDN pin= “L”.
- (2) The Internal regulator is powered up by bringing the PDN pin = “H” after operation clock is input. Then, SRC circuit is powered up and starts Ratio detection by ILRCK and OLRCK. SDTO is output after group delay period when Ratio detection is completed. Until then the SDTO outputs “L”. The time until SDTO output become enabled after setting the PDN pin to “H” is 9.6msec (Max.)

- (3) SDTO data output becomes enabled.
- (4) The statuses of the CM, ODIF and IDIF pins should be changed while the PDN pin= "L".

Case2: ILRCK and OLRCK are not input when the PDN pin= "H"

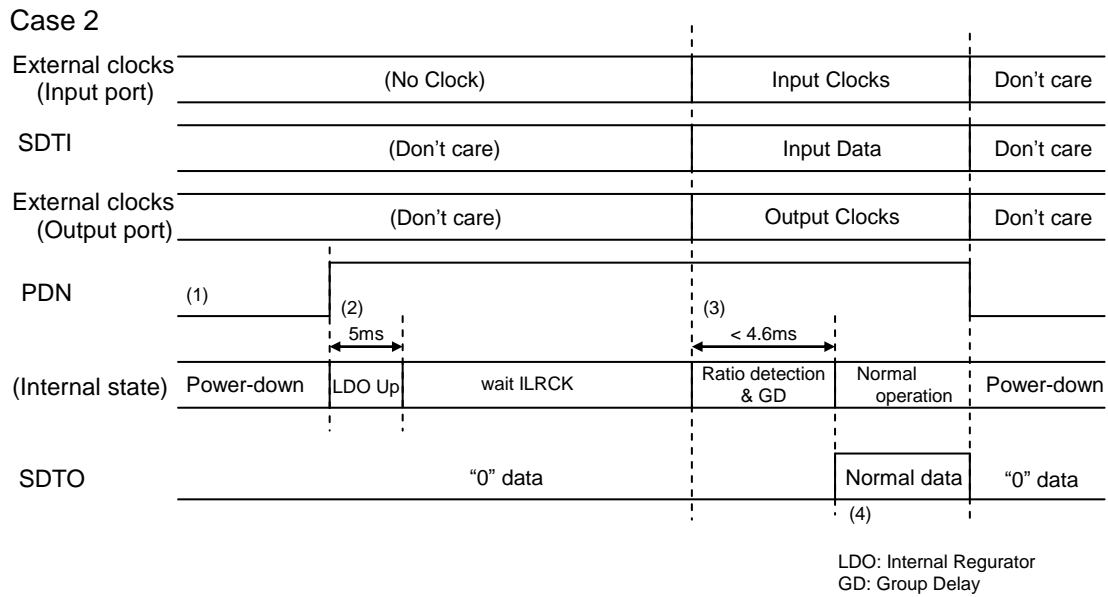


Figure 16. System Reset Case2

Note:

- (1) The SDTO pin output is "L" when the PDN pin= "L".
- (2) The internal regulator is powered up by PDN pin = "H" and wait for ILRCK and OLRCK.
- (3) SRC circuit is powered up and sampling frequency ratio detection starts when ILRCK and OLRCK are input. SDTO output starts after group delay period when the frequency ratio detection is completed. Until then, the SDTO output is "L". The time until SDTO output becomes enabled after ILRCK and OLRCK input is 4.6msec (Max.).
- (4) SDTO output becomes enabled.

## ■ Clock Switch Sequence

The AK4132 must be reset by bringing the PDN pin to “L” when changing operation clocks. Clock change sequence is shown in Figure 17.

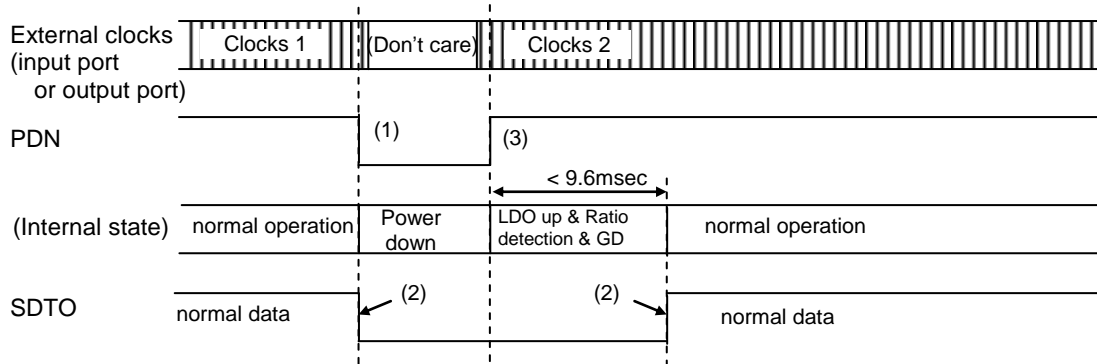


Figure 17. Clock Change Sequence

Note:

- (1) Set the PDN pin to “L”, and change clock frequencies of the IDIF pin, ODIF pin and CM pin.
- (2) The data on SDTO may cause a clicking noise.
- (3) Set the PDN pin to “H” after changing the clock of the IDIF pin, ODIF pin or CM pin.

The AK4132 has automatic internal reset function for when ILRCK or OLRCK frequency is changed. The behavior of the device when ILRCK or OLRCK frequency is changed is shown below.

- When the frequency of ILRCK at input port is changed without a reset by the PDN pin.

When the difference of internal oscillator clock number in one ILRCK cycle between before and after changing ILRCK frequency (FSO/FSI ratio should be stabilized) is more than 1/16 for 8cycles (\*), an internal reset is made automatically and sampling frequency ratio detection is executed again. SDTO outputs “L” when the internal reset is made, and SRC data is output after 162/FSI(O). (FSI(O) is lower frequency between FSI and FSO.)

When the above condition (\*) is not satisfied, the internal reset mentioned before will not be executed. It takes 5148/FSO (max. 116.7msec @FSO=44.1kHz) (Note 18) to output normal SRC data. Distorted data may be output until normal SRC output.

When ILRCK is stopped, an internal reset is executed automatically. It takes 162/FSI(O) to output normal SRC data after ILRCK is input again.

- When the frequency of OLRCK at output port is changed without a reset by the PDN pin

When the difference of internal oscillator clock number in one OLRCK cycle between before and after changing OLRCK frequency (FSO/FSI ratio should be stabilized) is more than 1/16 for 8cycles (\*), an internal reset is made automatically and sampling frequency ratio detection is executed again. SDTO outputs "L" when the internal reset is made, and SRC data is output after 162/FSI(O).

When the above condition (\*) is not satisfied, the internal reset mentioned before will not be executed. It takes 5148/FSO (max. 116.7msec @FSO=44.1kHz) (Note 18) to output normal SDTO data. Distorted data may be output until normal SDTO output.

When OLRCK is stopped, an internal reset is executed automatically. It takes 162/FSI(O) to output normal SDTO data after OLRCK is input again.

Note 18. When FSO/FSI ratio is changed from 1/6 to 1/5.99.

### ■ Grounding and Power Supply Decoupling

The AK4132 requires careful attention to power supply and grounding arrangements. Decoupling capacitors should be placed as near as possible to the supply pins.

### 14. Jitter Tolerance

Figure 18 shows the jitter tolerance to ILRCK and IBICK. The jitter quantity is defined by the jitter frequency and the jitter amplitude shown in Figure 18. When the jitter amplitude is 0.01U<sub>ipp</sub> or less, the AK4132 operates normally regardless of the jitter frequency.

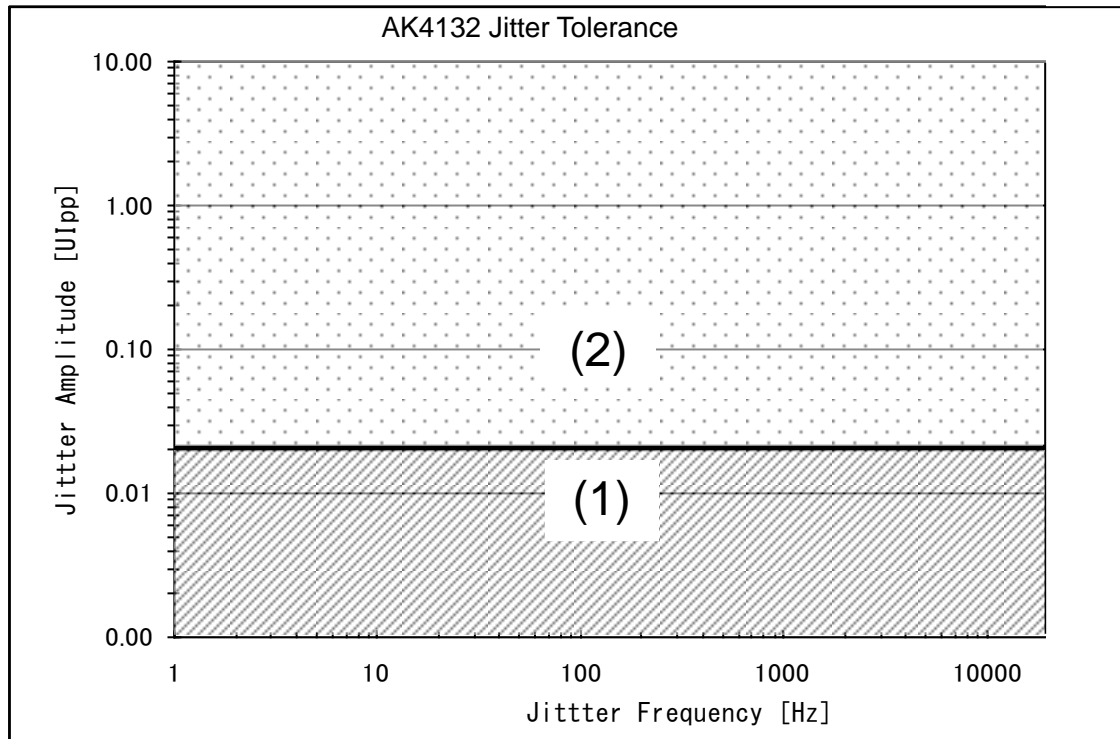


Figure 18. Jitter Tolerance

This is an evaluation result with synchronous input data to ILRCK and IBICK when jitter is added. The area (1) and (2) border is the the jitter amplitude of ILRCK just before THD+N degradation starts. Please use the jitter amplitude of the area (1).

- (1) Normal Operation
- (2) There is a possibility that the output data is lost.

1UI (Unit Interval) is one cycle of IBICK.  $1[\text{UIpp}] = 1/48\text{kHz} = 20.8\mu\text{sec}$  when FSI is 48kHz.

**15. Recommended External Circuits**

Figure 19 and Figure 20 show the system connection diagram.

- Regulator: Enable
- Output PORT: Master Mode

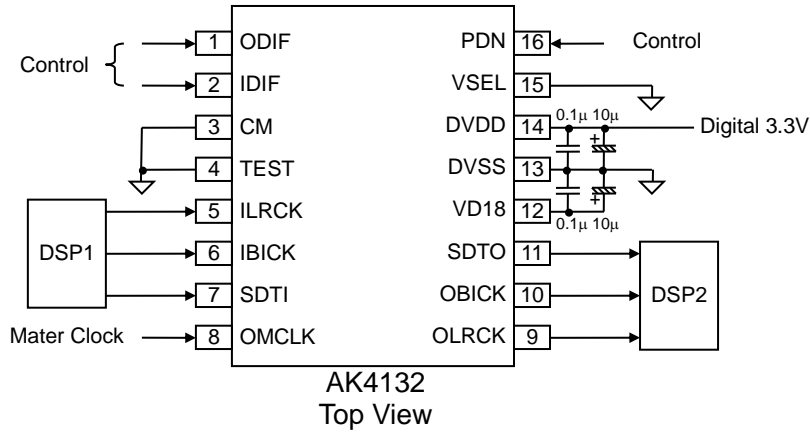


Figure 19. Typical Connection Diagram (Output Port: Master Mode, Regulator: Enable)

- Regulator: Disable
- Output PORT: Slave Mode

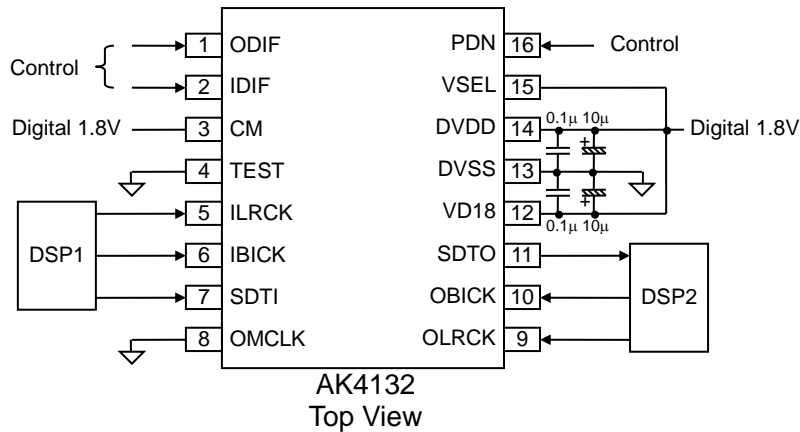
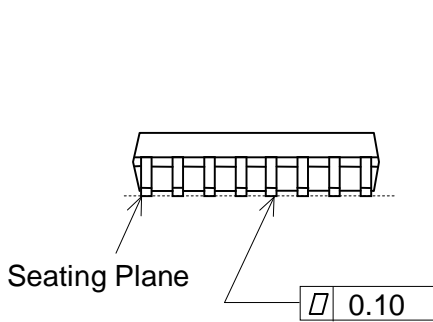
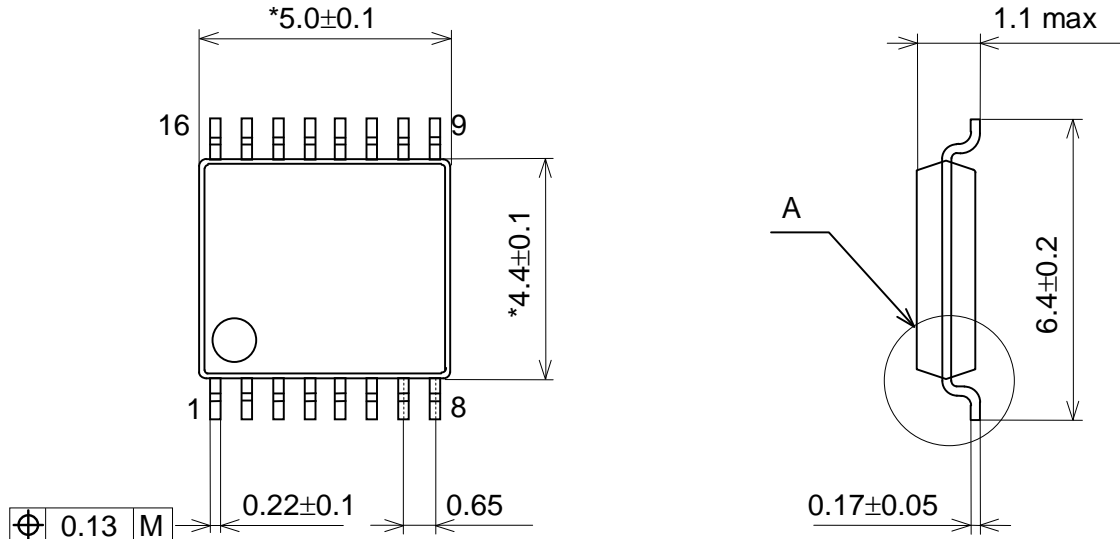


Figure 20. Typical Connection Diagram (Output Port: Slave mode, Regulator: Disable)

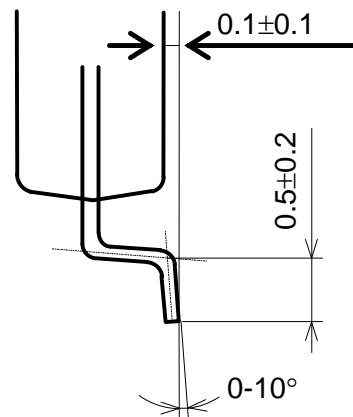
**16. Package**

■ Outline Dimensions

16-pin TSSOP (Unit: mm)



Detail A

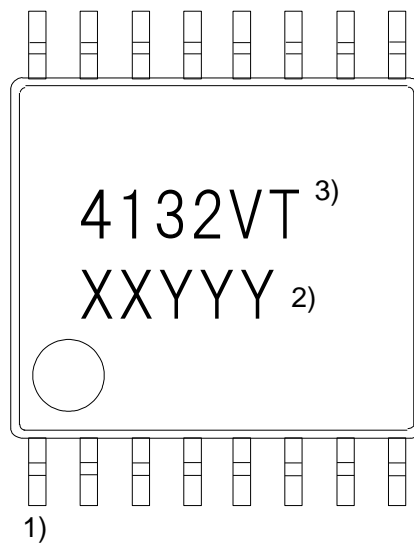


NOTE: Dimension "\*" does not include mold flash.

■ Material & Lead Finish

Package Molding Compound: Epoxy  
 Lead Frame Material: Cu  
 Pin Surface Treatment: Solder (Pb free) Plate

■ **Marking**



- 1) Pin #1 indication
- 2) Date Code : XXYYYY (5 digits)  
XX:Lot#  
YYY:Date Code
- 3) Marketing Code : 4132VT



**17. Ordering Guide**

AK4132VT      -40 ~ 105°C      16-pin TSSOP (0.65mm pitch)  
AKD4132      Evaluation Board for AK4132

**18. Revision History**

Date (Y/M/D)	Revision	Reason	Page	Contents
15/12/09	00	First Edition		

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